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Quarterly Technical Report

Solid State Research

2000:1

Lincoln Laboratory

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
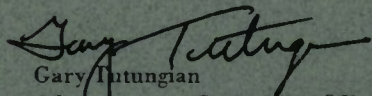
LEXINGTON, MASSACHUSETTS

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FOR THE COMMANDER

Gary Tutungian
Administrative Contracting Officer
Plans and Programs Directorate
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MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LINCOLN LABORATORY

SOLID STATE RESEARCH

QUARTERLY TECHNICAL REPORT

1 NOVEMBER 1999 — 31 JANUARY 2000

ISSUED 16 AUGUST 2000

LEXINGTON   MASSACHUSETTS

ABSTRACT

This report covers in detail the research work of the Solid State Division at Lincoln Laboratory for the period 1 November 1999 through 31 January 2000. The topics covered are Quantum Electronics, Electro-optical Materials and Devices, Submicrometer Technology, Biosensor and Molecular Technologies, Advanced Imaging Technology, Analog Device Technology, and Advanced Silicon Technology. Funding is provided by several DoD organizations—including the Air Force, Army, BMDO, DARPA, Navy, NSA, and OSD—and also by the DOE, NASA, and NIST.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

vii

LIST OF ILLUSTRATIONS (Continued)

LIST OF ILLUSTRATIONS (Continued)

LIST OF ILLUSTRATIONS (Continued)

LIST OF ILLUSTRATIONS (Continued)

LIST OF TABLES

INTRODUCTION

1. QUANTUM ELECTRONICS

Microchip-laser-pumped optical parametric generators packaged in 10-cm-long × 2.5-cm-diam stainless steel cans have been demonstrated, which convert the 1.064-μm output of the laser into radiation at preselected wavelengths between 1.4 and 4.3 μm with quantum efficiencies >40%, resulting in mid-ir pulses of <200-ps duration with peak signal powers >140 kW. The optical head includes a heater that can be used to temperature tune the devices over several 10s to 100s of nanometers.

2. ELECTRO-OPTICAL MATERIALS AND DEVICES

Avalanche photodiodes with multiplication gain up to ten in the 320- to 360-nm wavelength range have been demonstrated utilizing GaN grown by hydride vapor-phase epitaxy. The external quantum efficiency at unity gain is measured to be 35%.

Liquid surface tension has been used to pull semiconductor wafers to very close contact and strong bonding. The process has been analyzed, and criteria for surface tension, wafer flatness, and elasticity have been derived.

A strong correlation has been found between the surface step structure and phase separation in metastable GaInAsSb epitaxial layers grown by organometallic vapor phase epitaxy. A periodic step structure suggests minimal phase separation, while an aperiodic surface structure is associated with extensive phase separation.

3. SUBMICROMETER TECHNOLOGY

A high-resolution stereolithographic patterning technique has been developed for producing arbitrarily shaped three-dimensional structures on the microscale. The technique is unique in that it makes use of commercial photoresist materials and wafer coating techniques that have been specifically developed for the integrated circuit industry for high-resolution high-throughput lithography.

Optical waveguide fabrication techniques compatible with a silicon-on-insulator complementary metal oxide semiconductor (CMOS) process have been demonstrated. High-Q micro-ring channel dropping filters printed using 248-nm optical lithography show the robustness of the overall process for defining subwavelength-resolution coupling structures.

4. BIOSENSOR AND MOLECULAR TECHNOLOGIES

New classes of biological and chemical sensors require the generation of a stable and controllable bilayer lipid membrane (BLM) in a semiconductor-based substrate. Currently available analytical and experimental studies of BLM formation show that it is possible to form stable membranes having geometries compatible with those achievable by conventional micromachining and microfabrication technologies.

5.   ADVANCED IMAGING TECHNOLOGY

The thinned region of a charge-coupled device (CCD) has been deformed under pressure to a strain approaching 1%, and the device has been operated, reproducibly, in this strain state. The dark current of the CCD rises with strain, but all other operating characteristics are affected negligibly.

6.   ANALOG DEVICE TECHNOLOGY

A novel autocorrelation experiment has been designed and fabricated in a 2.0-V, 0.25-μm fully depleted silicon-on-insulator (FDSOI) CMOS circuit process, and used to measure the width of pulses emitted from a self-resetting pulse generator. The autocorrelator is a useful diagnostic tool in measuring the operation of the pulse generator, variations of which are employed in each pipeline stage of a subnanosecond asynchronous static random access memory (SRAM).

An asynchronous pipelined 8-kb (1 k $\times$ 8 b) SRAM integrated circuit with a 1.3-ns access time and 750-ps cycle time has been designed and fabricated in a 2.0-V, 0.25-μm FDSOI CMOS process, and tested by clocking it at a cycle rate of 10 MHz. Data bytes can be reliably stored into and recalled from most of the 1000 8-b address locations on the circuit.

7.   ADVANCED SILICON TECHNOLOGY

The dark-field phase-shift mask method has been extended to the chromeless regime, achieving lithography with good process latitudes down to k1 = 0.13 for isolated features and k1 = 0.3 for dense features. An advanced polysilicon etch process has also been developed that has obtained successful pattern transfer for gate features down to 25 nm, near the physical limits of CMOS functionality.

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xvii

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Antimonide-Based Mid-IR Semiconductor Lasers	H. K. Choi	Technical Seminar, Massachusetts Institute of Technology, Cambridge, Massachusetts, 17 November 1999
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157-nm Resist Fundamentals	T. H. Fedynyshyn R. R. Kunz	157-nm Data Review Meeting, Waltham, Massachusetts, 18-19 November 1999

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[†] Titles of presentations are listed for information only. No copies are available for distribution.

157-nm Resist Update from Lincoln Laboratory	R. R. Kunz T. H. Fedynyshyn	157-nm Data Review Meeting, Waltham, Massachusetts, 18-19 November 1999
Optical Materials at 157 nm Lithography	M. Rothschild	157-nm Data Review Meeting, Waltham, Massachusetts, 18-19 November 1999
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Magnetically Tuned Superconducting Filters	D. E. Oates A. C. Anderson	1999 Fall Meeting of the Materials Research Society, Boston, Massachusetts, 29 November– 3 December 1999
Microstructural Characterization of Antimonide Based III-V Compounds and Their Effect on Electro-Optical Properties of Substrate Materials and Devices	C. A. Wang P. S. Dutta* R. J. Gutmann* G. W. Charache*	1999 Fall Meeting of the Materials Research Society, Boston, Massachusetts, 29 November– 3 December 1999

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1. QUANTUM ELECTRONICS

1.1 MINIATURE SOURCES OF SUBNANOSECOND 1.4–4.3-μm PULSES WITH HIGH PEAK POWER

In 1997, Zayhowski demonstrated that periodically poled lithium niobate (PPLN) optical parametric generators (OPGs) can be used to efficiently convert the subnanosecond output of a high-power 1.064-μm microchip laser into radiation at wavelengths between 1.4 and 4.3 μm [1]. Shortly thereafter, the same author reported bulk KTP optical parametric oscillators (OPOs) pumped with the second harmonic of the microchip laser output [2],[3]. More recently, Bäder et al. used a frequency-doubled Nd:YAG source to pump PPLN OPGs operating at signal wavelengths between 637 and 593 nm [4]. Although all of these works demonstrated the feasibility of extremely compact and robust optical parametric systems, none of the reports indicate that the authors actually produced such a device—the authors reported laboratory experiments. Here, we report on the construction and characterization of a mid-ir microchip-laser-pumped OPG packaged in a 10-cm-long × 2.5-cm-diam stainless steel can. The optical head, shown in Figure 1-1, contains the fiber-pumped microchip laser, the OPG, and an oven to control the temperature of the OPG between 100 and 165°C. The output consists of sub-200-ps mid-ir pulses (2.5× shorter than previously reported) with peak signal powers >140 kW (70% higher than previously reported), corresponding to quantum conversion efficiencies from the pump to signal and idler wavelengths of >40% (60% better than in our previous experiments [1]). The nominal output wavelength (including signal and idler) can be selected to be anywhere between 1.4 and 4.3 μm, and can be tuned over several 10s to 100s of nanometers with a bandwidth of a few nanometers.

The 1.064-μm passively Q-switched microchip laser used to pump the OPG is similar to a device described elsewhere [5],[6]. It has a total cavity length of 6.5 mm and is pumped with the fiber-coupled output of a 10-W diode laser array. Its output consists of 98-μJ pulses with a full width at half-maximum (FWHM) of 400 ps. The laser oscillates in a single longitudinal mode with a linearly polarized, diffraction-limited output beam. The $1/e^2$ beam radius at the output facet of the laser is ~70 μm; the peak optical intensity exiting the facet is 2.7 GW/cm^2. This laser has a shorter pulse and higher peak power than the pump laser used in previous demonstrations, leading to the enhanced performance of the OPG described above.

The laser chip is mounted on a gold-coated copper base. The output of the laser exits a stainless steel cover through a lens. After passing through the lens (discussed below), it enters an oven containing the PPLN. The 2-cm-long oven comprises two blocks of gold-coated copper, fastened together. The top block has a 1-cm-wide × 1-mm-high trough cut in it to accommodate the PPLN. The PPLN is epoxied to the bottom block with an appropriately selected compliant, high-temperature epoxy. (The thermal expansion coefficient for copper, 16.6×10^{-6}/°C, is well matched to the thermal expansion coefficient for lithium niobate in the plane normal to the c-axis, 15.4×10^{-6}/°C.) The trough containing the PPLN runs along the optic axis of the device with the laser light entering at one end and exiting the other. The oven is supported

1

Figure 1-1. Photograph of optical head of a microchip-laser-pumped periodically poled lithium niobate optical parametric generator (OPG) with OPG cover removed.

by the same stainless steel structure that covers the microchip laser and holds the lens. The stainless steel has been machined to provide high thermal impedance between the oven and the rest of the structure, while still being sufficiently rigid to form a robust package. A 10-W resistor mounted on the top copper block of the oven is used to heat the oven; a thermistor on the bottom is used to monitor the oven temperature. The thermistor forms one arm of a Wheatstone bridge used to control the current to the resistor, regulating the oven temperature to within 1°C at temperatures between 100 and 165°C. The power required to maintain the oven, and the PPLN within it, at 165°C is slightly less than 10 W. The oven is easily seen in the center of Figure 1-1. The cover to the oven, in the lower right part of Figure 1-1, has an outer diameter of 2.5 cm, and brings the total length of the optical head to 10 cm.

As discussed above, the 1.064-μm output of the microchip laser passes through a lens before entering the PPLN. The lens has a focal length of 11 mm. Initially, the lens was positioned to image the output facet of the microchip laser 1-to-1 in the center of a 2-cm-long piece of PPLN. The PPLN contained 14 gratings, with periods of 28.2, 28.5, 28.7, 28.9, 29.1, 29.3, 29.5, 29.7, 29.9, 30.2, 30.4, 30.6, 30.8, and 31.0 μm. When pumped at 1.064 μm at a nominal temperature of 140°C, these gratings generate signal wavelengths between 1.46 and 1.84 μm, and idler wavelengths between 2.52 and 3.91 μm. The input and output facets of the PPLN are broadband antireflection coated. All of the gratings were tested at a pulse repetition rate of 500 Hz with the lens in its initial position. Each resulted in ~45% quantum conversion efficiency of the incident pump light to the output signal and idler wavelengths, as determined from pulse-energy measurements. The exact conversion efficiency, between 43 and 47%, was more a function of the amount of time spent "tweaking" the crystal than the grating used.

The optical intensity of the pump light in the PPLN with the lens in its initial position, 2.7 GW/cm^2, was more than the PPLN could sustain without damage. After a short period of operation, small pits were blown out of the material about 8 mm from the input facet of the PPLN, near the focus of the pump light. This caused the crystal to crack, rendering all of the gratings useless.

All further measurements were made on a 17-mm-long piece of PPLN with the lens ~10 mm from the output facet of the laser. With the lens in this position, the pump light continued to diverge slightly after passing through the lens, and the maximum pump intensity in the crystal was estimated to be <1.5 GW/cm^2. At this intensity, we saw no evidence of damage to the crystal with our 400-ps-long pump pulse. The grating in the PPLN has a 29.5-μm period. Based on previous experience, we believe that the results obtained with this grating are representative of what can be expected for gratings covering the spectral region from 1.4 to 4.3 μm.

Despite the lower pump intensity and shorter crystal length, the 17-mm-long PPLN operated with a quantum efficiency of 41%, producing 28.5 and 12.4 μJ at the signal and idler wavelengths, respectively. This measurement was made at an oven temperature of 140°C, but is typical of the performance at any temperature between 23 and 165°C, as long as there is no photorefractive damage. We observed no photorefractive damage at room temperature. As the crystal was heated toward 100°C, the amount of parasitic green light generated increased and photorefractive damage was observed. Between 100 and 165°C (the temperature range of our oven) the OPG operated free of photorefractive damage. In the absence of photorefractive damage, the output was diffraction limited.

The output spectrum of the OPG signal was measured as a function of oven temperature; the spectrum of the idler was inferred from these measurements. The results are summarized in Figure 1-2. The center wavelength of the signal tuned from 1.495 μm at room temperature to 1.542 μm at 160°C. The spectra were more or less Gaussian, with a FWHM between 7 and 8 nm. The corresponding idler wavelength tuned from 3.691 to 3.432 μm, with a FWHM between 45 and 40 nm.

The signal had a measured pulsewidth of 180 ps, FWHM. Again, this measurement was made at an oven temperature of 140°C, but is typical of measurements made at other temperatures as well. As has been previously observed [2], the power at the temporal peak of the pump pulse is nearly 100% converted to the signal and idler wavelengths. The peak power at the signal wavelength is ~140 kW; the idler has a peak power of ~60 kW.

We have demonstrated a compact, robust, microchip-laser-pumped PPLN OPG system whose optical head measures 2.5 cm in diameter by 10 cm in length. This device can be constructed to operate in a preselected wavelength region between 1.4 and 4.3 μm, with a tunability of several 10s to 100s of nanometers. The mid-ir output has a FWHM of <200 ps, with peak powers, at the signal wavelength, of >100 kW. Potential applications include high-resolution eye-safe ranging and three-dimensional imaging using time-of-flight techniques, ir matrix-assisted laser desorption and ionization, and spectroscopy.

J. J. Zayhowski
A. L. Wilson, Jr.
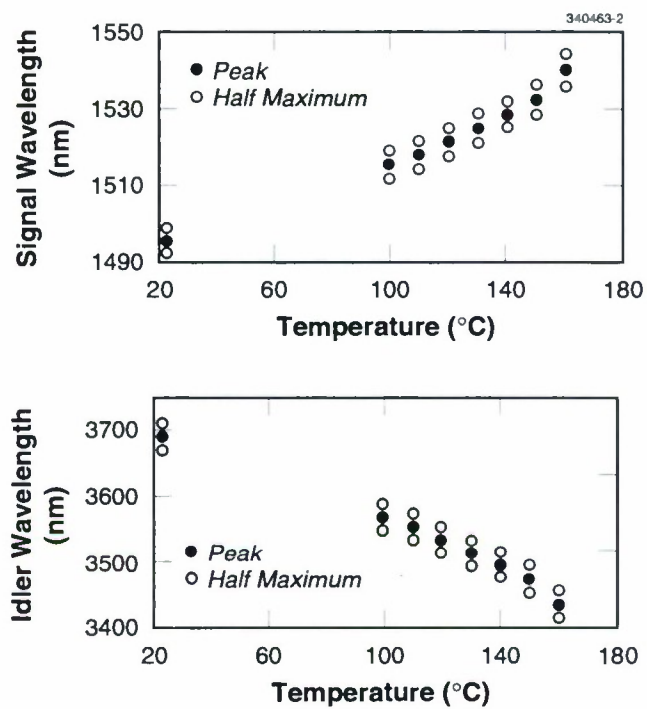
Figure 1-2. OPG signal and idler wavelength as a function of oven temperature.

4

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2. ELECTRO-OPTICAL MATERIALS AND DEVICES

2.1 GaN AVALANCHE PHOTODIODES GROWN BY HYDRIDE VAPOR-PHASE EPITAXY

GaN and AlGaN material and device technology has developed quickly in the past several years, leading to major advances in the state of the art for sources and detectors in the short-wavelength visible and uv bands [1],[2]. Both metal-semiconductor-metal [3],[4] and photodiode [5]–[7] detectors have been reported in GaN. The development of GaN avalanche photodiodes (APDs), however, has been hampered by the formation of microplasmas due to defects in the material [8]. This report describes the demonstration of APDs with spatially uniform gain regions free of microplasmas, work that has been enabled by the high quality of the GaN films grown by hydride vapor-phase epitaxy (HVPE).

All of the GaN layers incorporated in these devices were grown in a vertical chloride-transport HVPE reactor. Details of the GaN growth are described elsewhere [9]. The photodiode structure is shown in Figure 2-1. A thin ($\sim$0.25 μm) Zn-doped layer was grown on top of a 10- to 15-μm-thick unintentionally doped ($\sim 10^{17}$ cm^{-3} n-type) GaN layer. The Zn-doped layer was produced by the introduction of diethylzinc in the reactor for the last 15 s of growth. Analysis by secondary ion mass spectrometry revealed a Zn concentration in the low 10^{19} cm^{-3} in the Zn-doped region. In HVPE GaN, Zn doping is believed to introduce an acceptor level at $\sim$340 meV above the valence band edge, resulting in p-type material [10]. After growth, mesas were dry etched with a range of diameters from 30 to 60 μm, and a SiO$_2$ passivation layer was deposited uniformly over the top of the wafer. Vias were opened to allow electrical contact to the center of the device. A thin semitransparent Ni or Ti electrode was defined on the top of the mesa, in order to uniformly contact the central region of the device. Finally, a thicker Au cathode was patterned in the ring shape shown in black in the lower half of Figure 2-1. An alloyed In anode made electrical contact to the n-type GaN.

A voltage source in series connection with a 200-kΩ load resistor biased the devices. Both forward and reverse electrical characteristics were measured. At small reverse bias voltages for a 37-μm-diam device, the measured dark current is at the limit of the measurement system ($\sim$100 fA). A leakage current of 100–200 nA is typically observed at voltages near –150 V. At a bias near –200 V, leakage current begins to increase more quickly, so that the load-line limit is reached near –250V. The current through the device is converted to a voltage with a 10^6-V/A transimpedance amplifier (TIA) whose output is fed to an oscilloscope or a lock-in amplifier during optical measurements.

Spatial uniformity and efficiency of optical response are measured by top illuminating the device with the focused beam from a cw HeCd laser at 325 nm. Since all of the power in the beam is confined to a spot ($<$5 μm diam) much smaller than the central area of the device, this allows an accurate measurement of the external quantum efficiency (EQE) at 325 nm. In order to determine the spatial uniformity of optical response in the device, the beam is scanned across the device in one dimension with a raster mirror and the device is translated in the orthogonal direction with a computer-controlled translation stage. A typical

7

Semitransparent
Ti Window (5 nm)
Au Cathode   Zn-doped p Layer (0.25 μm)
In Anode   SiO$_2$ (0.5 μm)

n-GaN Layer (10 μm)

Side View   Sapphire Substrate
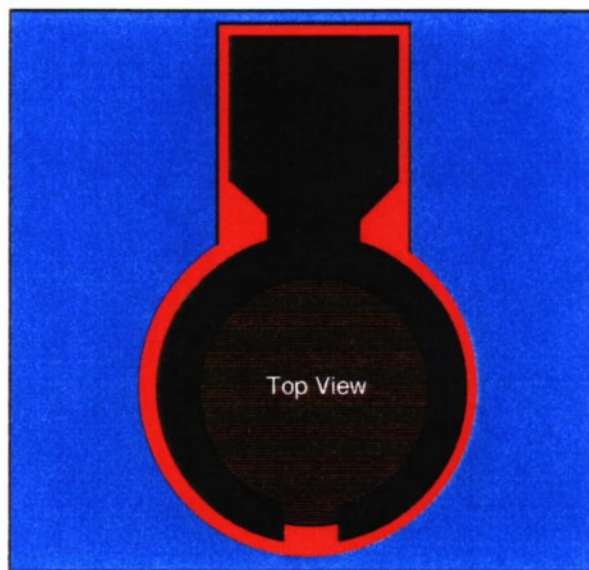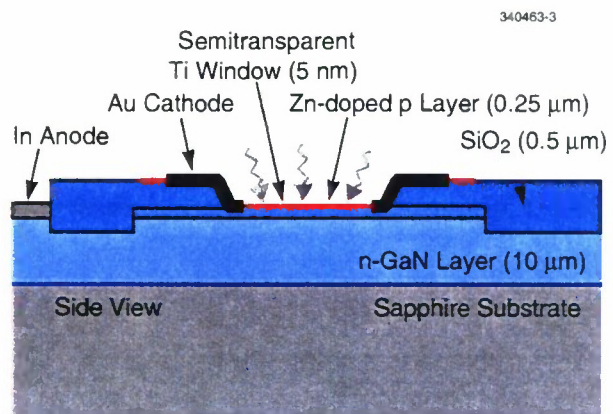
Top View

Figure 2-1. Cross-sectional and top-view drawings of the GaN avalanche photodiode structure.

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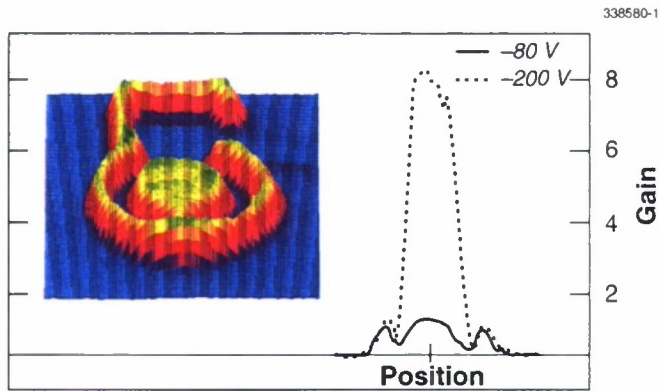
Figure 2-2. Two-dimensional raster image of photocurrent at –30-V bias is shown on left; response is uniform from all regions on the mesa not covered by the opaque Au layer. On the right, photoresponse raster slices through the mesa center are shown for two bias voltages; multiplication gain of ~8 is found to occur uniformly in the central region of the mesa at –200 V.

low-voltage (–30 V) raster image is shown in the left side of Figure 2-2, where optical response occurs everywhere on the mesa that is not blocked by the opaque Au contact. This includes the thin area on the mesa outside the Au, even though that region is not directly contacted by the Ti layer. The Ti makes contact with the GaN only inside the hole etched in the passivation layer. The edges of the Ti and Au metal arc over the passivation layer, thus mitigating the electric field enhancement that usually occurs at the edges of a planar electrode. This was essential for achieving a spatially uniform gain region. No optical response was found outside the mesa.

The right side of Figure 2-2 shows raster curves, measured from left to right through the center of a 37-μm-diam mesa, recorded for two reverse bias voltages. The lower curve (–80 V) corresponds to a voltage where unity-gain response is found uniformly across the device. As the voltage is increased, within the central region of the device a uniform gain is observed. Results shown here are typical of this type of device, exhibiting a uniform multiplication gain of ~8 at –200 V (upper curve). A maximum gain of 10, corresponding to an EQE of 350%, was measured at just below their breakdown voltage (–220 V) in these devices. These results are a clear indication of the onset of avalanche gain in our HVPE-GaN photodiodes.

One of the problems typically faced when developing APDs is nonuniform avalanche breakdown or microplasma formation caused by local field enhancement at defects in the material. We have observed this type of behavior in some devices, where, above a threshold voltage and at sufficiently high currents, visible emission can be observed from the microplasma with a video camera used to monitor the device during testing. In addition, locally enhanced photoresponse can be seen at the sites of some of those defects. In low-defect-density passivated devices, microplasma formation and nonuniform gain are

9

reduced or eliminated completely. Devices with no visible microplasma behavior were used to obtain the data shown here.

The spectral dependence of the photoresponse was measured with a Xe-arc lamp source coupled to a 0.5-m grating monochomator. The relative response is calibrated with a large-area uv-enhanced Si detector, and the absolute responsivity is calibrated at 325 nm, as discussed previously. Typical spectral response curves are shown in Figure 2-3. The peak response at 362 nm, corresponding to the room-temperature band gap energy of GaN, and the sharp drop in response below the band edge at low voltages are indications of the high quality of the HVPE GaN. A reduction in response at wavelengths shorter than 350 nm at low voltage is representative of the reduced collection efficiency typically found in a GaN "deep junction" when the light is absorbed near the top p-type surface of the material. As bias is increased from 0 to –50 V this roll-off in response between the band edge and 320 nm is eliminated, since the collection efficiency increases most strongly for those carriers generated near the top surface of the device (shortest wavelengths). Above –60 V, photoresponse is only weakly dependent on wavelength between 320 and 360 nm. The apparent roll-off in response at wavelengths shorter than 320 nm may be caused by instrumentation error. At a bias between –60 and –80 V, unity gain is achieved in the device. The measured unity-gain EQE is ~35% at 325 nm and is limited partly by reflection from the thin Ti electrode and the GaN, which transmit <50% of the incident radiation. As seen in Figure 2-3, an avalanche gain of 10 is produced as the bias is increased from –60 to –220 V for this device. Shown in the inset to Figure 2-3 is the voltage dependence of the photocurrent at 350 nm, clearly indicating the transition from low voltage behavior (increasing collection efficiency) to high voltage behavior (multiplication gain) near –80 V.

The increase in photoresponse observed below the band edge at high bias voltages is consistent with Franz-Keldysh absorption in the high-field portion of the device. The slope of the high-voltage curves below the band edge indicates an electric field strength of greater than 1.5 MV/cm, in rough agreement with high voltage capacitance-voltage (C-V) data recorded from these devices. The electric field found from C-V measurements at a bias voltage near the onset of avalanche gain (1.6 MV/cm) is in good agreement with that predicted for electron-initiated avalanche breakdown in GaN [11]. Electric fields as high as 4 MV/cm have been measured in these devices. One of the ongoing improvements to these devices will be the use of a separate absorption and multiplication structure, which will allow us to eliminate the high electric field in the absorption region of the device and thus retain excellent rejection of below band gap light at high voltage.

Measurements of the speed of response of these photodiodes were made by mechanically chopping the beam from the HeCd laser at a beamwaist between a pair of lenses. When a device is illuminated with this source, the falling edge of the detector photocurrent on an oscilloscope is found to have a 90–10% fall time of <5 μs. This measurement is limited by the bandwidth of our transimpedance amplifier; if the speed of response is limited by the resistance-capacitance decay time of the device, it would be expected to be <10 ns. Note that the above type of measurement is much more sensitive to long time-constant effects than measurements made with short optical pulses.
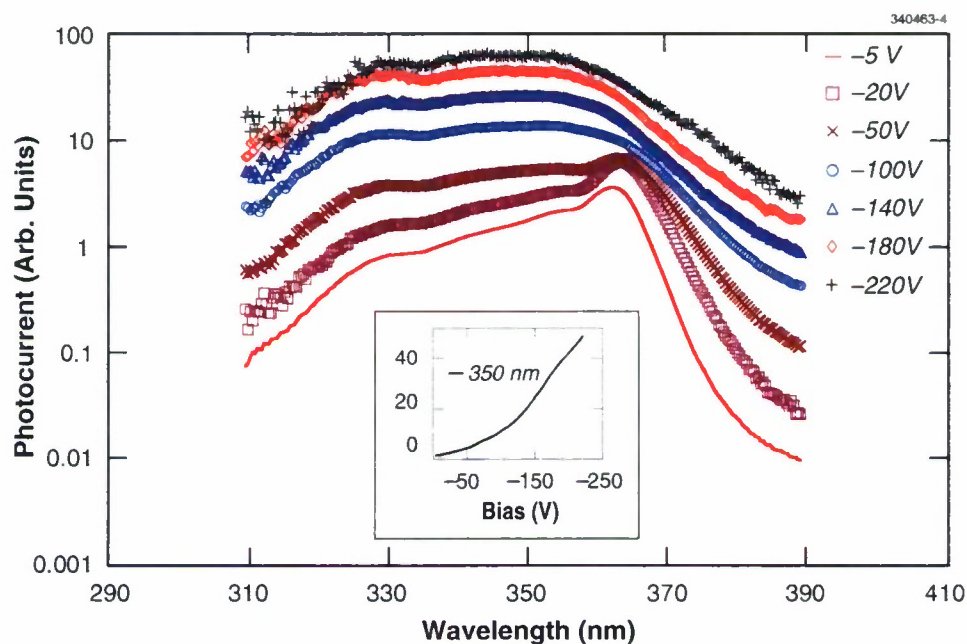
Figure 2-3. Spectral dependence of the photoresponse is shown. Unity gain is found to occur at voltages between –60 and –80 V from 320 to 360 nm. A multiplication gain of 10 is measured at –220 V. The inset plots the bias dependence of the photocurrent for a wavelength of 350 nm.

We have reported the demonstration of GaN APDs with a spatially uniform gain region. These HVPE-grown GaN APDs exhibited maximum multiplication gains of 10. Multiplication gain was found to be independent of wavelength from 320 to 360 nm. The response time of these photodiodes was measured to be <5 μs.

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11

2.2 WAFER BONDING VIA LIQUID SURFACE TENSION

There has been considerable interest in wafer bonding [12] and wafer fusion [13]–[20] for integration of dissimilar semiconductor materials, devices, and systems. Mechanical pressing is widely used to force wafers into contact. Pulling by liquid surface tension has also been inferred by several authors [12],[14]. In this report, we describe investigations of the mechanics of surface-tension pulling and develop a simple analytical model for the process. We demonstrate that surface tension can effectively pull wafers to a uniform atomic contact.

Experiments were first carried out by using wafer couples of the combinations of GaP, GaAs, InP, Si, and sapphire. Most wafer surfaces were polished, but some had grown epitaxial layers. In each run, the wafers were thoroughly cleaned (often lightly etched), rinsed in methanol, and then assembled wet. (Methanol wet all materials used in the present work, indicating relatively strong adhesive forces.) Evaporating through the openings along the edges, the methanol between the wafers became thinner and eventually pulled the latter to contact. This process can be conveniently monitored by watching the interference fringes of the liquid thin film from the top surface of a transparent wafer (GaP or sapphire). The fringes gradually pushed out, and eventually the entire wafer area became fringeless except for occasional difficult spots. The fringeless condition indicates a wafer separation less than a quarter of the visible wavelength, or ~1000 Å. For centimeter-sized wafers, this condition was usually reached in ~0.5 h. Since additional time is presumably needed for the remaining 1000 Å of methanol to completely escape, several more hours were allowed in order to achieve the best atomic contact between wafers.

The average air gaps between some bonded GaP wafers were measured by evanescent-wave tunneling and showed a meager 15 Å, indicating a very close contact limited probably only by the atomic steps of the wafer surface. Indeed, the wafers were firmly held together by molecular force and would not separate even after being submerged in methanol in ultrasonic vibration for several hours. Some bonded wafers were placed in a furnace for heat treatment in H_2 up to 1010°C. Heat-treated GaAs/GaAs and GaP/GaP showed ohmic conduction across the interfaces, indicative of wafer fusion. Bonded Si/(InGaAs/InP) were heat treated to 500°C to fuse InGaAs to Si. It is worth noting that no pressure was applied during the heat treatment but the bonded wafer couples remained together despite considerable thermal stress between dissimilar materials, especially Si and InP.

The bonding strength, however, seemed to vary, depending on the wafer material, surface, elasticity and adhesive forces. A comprehensive modeling of the surface-tension pulling is therefore desirable for better process control.

The wafer surfaces are generally not entirely flat, having various degrees of curvature or waviness. In the present model, we first consider a simple basic case of a thin flat plate and a convex surface, as illustrated in Figure 2-4. To conform, a pair of forces F can be applied to elastically deform the plate. This puts the upper and lower halves of the plate in tensile and compressive strains, respectively. Let ε and $-\varepsilon$ be the average strains of the two portions. It then follows from the geometrical relationships.

12

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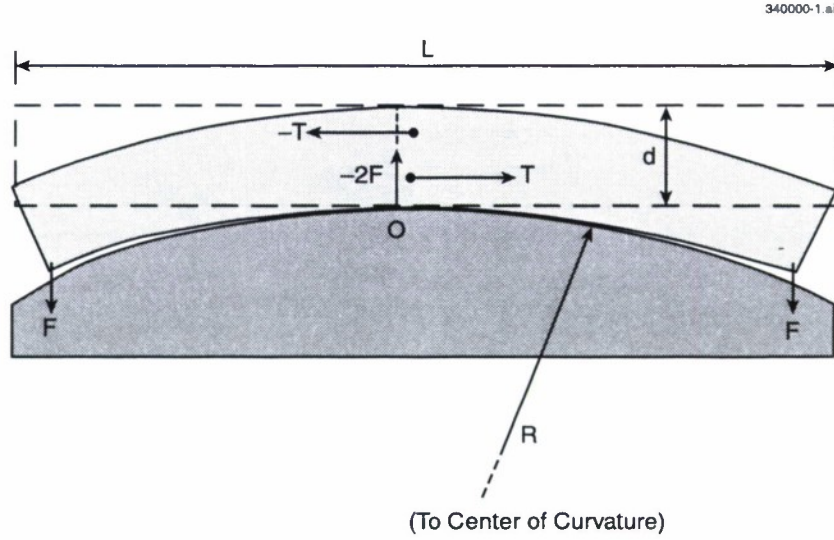
Figure 2-4. Bending of a flat wafer, by applied forces F, to conform to an underlying wafer with a curved surface. The upper and lower halves of the elastically deformed wafer are under tensile and compressive strains, respectively, and –T and T illustrate the corresponding stress forces acting on the right half of the wafer by the left half.

$$\varepsilon = \frac{d}{4R} , \qquad (2.1)$$

where R is the radius of curvature of the surface and d is the thickness of the plate. The corresponding stress force T is given by [21]

$$T = \frac{EWd^2}{8R} , \qquad (2.2)$$

where E is the Young's modulus of the plate material, W is the width of the plate (perpendicular to the page). Now consider only the right half of the plate. The stress forces T and $–T$ exert a torque τ to that half of the plate. Choosing the origin O to be the reference point, we have

$$\tau = Td/2 . \qquad (2.3)$$

At mechanical equilibrium, this torque is to be countered by that produced by the applied force F, i.e.,

13

$$F = Td/L$$

$$= \frac{EWd^3}{8RL} \, , \tag{2.4}$$

where L is the length of the plate. ($L/2$ is the moment of the force F with respect to the origin O.) Note that generally $d \ll L$ and hence $F \ll T$. Also, F has a very strong dependence on d.

An equivalent of the pulling force F can be produced by surface tension when a liquid is present, as illustrated in Figure 2-5. The adhesive force between the liquid and the solid surfaces establishes a meniscus near each end of the plate. The surface tension of the liquid then produces a hydrostatic pressure [22]

$$P = 2\alpha/\Delta \, , \tag{2.5}$$

where α is the coefficient of surface tension and Δ is the separation of the solid surfaces. Since the radius of curvature R is usually much greater than the wafer dimension L, we have

$$\Delta \cong \frac{L^2}{8R} \, . \tag{2.6}$$

To be able to bend the plate, we set

$$\int_0^{L/2} x \ PW \ dx \ > \ \tau \, , \tag{2.7}$$

where τ is the torque given by Equation (2.3). Equation (2.7) can then be integrated and rearranged to yield

$$\alpha \ > \ \frac{Ed^3}{32R^2} \, , \tag{2.8}$$

as the required strength of the surface tension. Note that it depends strongly on both the wafer thickness d and the radius of curvature R. Consider a set of parameters, $d = 200 \, \mu m$, $E = 1 \times 10^{12} \, dyne/cm^2$ [23], and $R = 1000$ cm (which corresponds to $\Delta = 1.25 \, \mu m$ for $L = 1$ cm). Equation (2.8) yields $\alpha > 0.25$ dyne/cm, a condition satisfied by the coefficient of surface tension of methanol $\alpha_{methanol} = 25$ dyne/cm [24]. This shows that surface tension is indeed capable of pulling wafers of moderate curvatures together.

For wafers of greater surface waviness or roughness, however, each local bump can have a relatively small radius of curvature R and the surface tension may not have the strength needed. It is nonetheless worth noting that the surface-tension effect grows larger when the gap Δ becomes smaller as can be seen in Equation (2.5). Thus, with some initial help to reduce the gap Δ, the effectiveness of surface tension can be enhanced. Indeed, experimentally we found that the process yield was increased by applying a moderate pressure by vise pressing during the drying period.

14
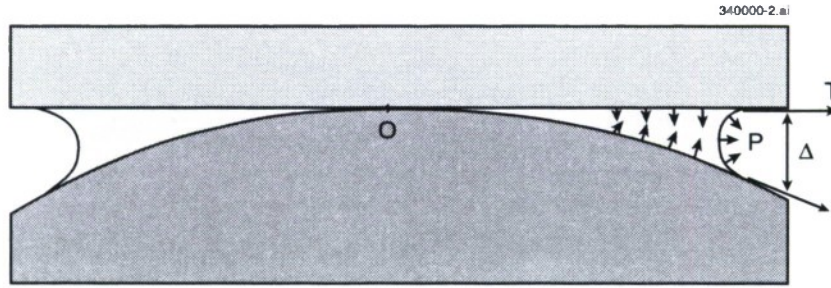
Figure 2-5. Illustration of the liquid surface tension that can pull two wafers into conformation.

We have demonstrated that surface tension is capable of pulling wafers to uniform close contact, which is otherwise not easily achievable by mechanical pressing with rigid anvils. This is a potentially useful technique for which our analytical model provides some simple guidance for implementation.

Z. L. Liau

2.3 CORRELATION BETWEEN SURFACE STEP STRUCTURE AND PHASE SEPARATION IN EPITAXIAL GaInAsSb

GaInAsSb alloys are of interest for lattice-matched thermophotovoltaic (TPV) devices because of the high performance attainable at 2.3–2.5 μm [25]. However, the GaInAsSb quaternary alloys exhibit a miscibility gap [26], and epitaxial layers can exhibit phase separation [25],[27]. Phase separation has been reported in numerous III-V systems [28] and leads to degradation in materials properties. It is associated with microscopic compositional inhomogeneity, which gives rise to contrast in transmission electron microscopy (TEM) images, reduced electron mobility [29], and broadening of both photoluminescence (PL) spectra [27],[30]–[31] and x-ray diffraction curves [27],[30]. Thus, it is of interest to understand the mechanism by which phase separation occurs.

It is generally believed that phase separation evolves at the epitaxial surface [32], which is reasonable because bulk diffusion coefficients of the constituent elements are too low to account for the length scales associated with phase separation observed in TEM. Thus, surface diffusion and adatom lifetime before incorporation into the lattice are expected to influence phase separation. In this report, the importance of the step structure of GaInAsSb, studied by atomic force microscopy (AFM), on phase

15

separation is demonstrated. Using 4-K PL spectra to evaluate the degree of phase separation, we find a strong correlation between the PL data, the step structure, and the length of surface terraces.

$Ga_{1-x}In_xAs_ySb_{1-y}$ ($0.1 < x, y < 0.2$) epitaxial layers, nominally lattice matched to GaSb, were grown by organometallic vapor-phase epitaxy in a low-pressure vertical rotating-disk reactor with trimethylindium, triethylgallium, tertiarybutylarsine, and trimethylantimony as precursors [27]. The growth temperature was varied between 525 and 575°C. At these growth temperatures, the GaInAsSb alloys grown are predicted to be metastable, and penetrate further into the miscibility gap with increasing x- and y-values [26]. The growth rate was varied between 1.2 and 5 μm/h. The substrates used were (001) GaSb substrates with miscut angles of 2° toward (101) or 6° toward ($1\bar{1}1$) B. AFM operated in tapping mode was used to study the surface step structure. PL measurements were performed at 4 and 300 K using 647=nm krypton laser excitation and a PbS detector.

AFM images and cross-section profiles, shown in Figure 2-6, indicate that the step structure is dependent on both growth temperature and alloy composition. Figures 2-6(a) and 2-6(b) show results for $Ga_{1-x}In_xAs_ySb_{1-y}$ epilayers grown on (001) 2° toward (101) GaSb substrates at 525°C with $x = 0.16$, $y = 0.15$, and at 575°C with $x = 0.12$, $y = 0.10$, respectively. The surface of the epilayer grown at 525°C is vicinal and consists of steps that are predominately one monolayer (~0.3 nm) high. On the other hand, the surface of the epilayer grown at 575°C is step bunched and consists of multilayer steps that are about 1.5 nm high. The terrace lengths for the epilayer grown at 575°C are about 39 nm, or nearly 5 times longer than those of the epilayer grown at 525°C. The root-mean-square (rms) roughness of the epilayer grown at 525°C is 0.2 nm compared to 0.6 nm for the layer grown at 575°C. Figure 2-6(c) shows the AFM scan for $Ga_{0.86}In_{0.14}As_{0.12}Sb_{0.88}$ grown at 575°C on a GaSb substrate of similar orientation. No periodic step structure is observed, and the surface exhibits deep crevices across the sample. The rms roughness of the surface is greater than 1 nm.

PL spectra from epilayers of Figure 2-6 are shown in Figure 2-7. The 300-K PL peak wavelength increases for larger x- and y-values, as expected. The full width at half-maximum (FWHM) of 4-K PL spectra is only 5.5 meV for $Ga_{0.84}In_{0.16}As_{0.15}Sb_{0.85}$ grown at 525°C [Figure 2-7(a)] and increases to 11.2 meV for $Ga_{0.88}In_{0.12}As_{0.1}Sb_{0.9}$ grown at 575°C [Figure 2-7(b)]. Even though the x- and y-values for the sample in Figure 2-7(a) are greater than those for the sample in Figure 2-7(b), the FWHM value is smaller, which suggests a lower degree of phase separation [27],[30]. The difference between the 4- and 300-K PL peak energy for both samples is about 0.07 eV, in line with the expected difference. In contrast, $Ga_{0.86}In_{0.14}As_{0.12}Sb_{0.88}$ grown at 575°C [Figure 2-7(c)] exhibits anomalous behavior. The 4-K PL peak energy compared to that at 300 K is red shifted. In addition, both 4- and 300-K PL spectra are greatly broadened, with PL intensity observed as far out as 2800 nm. Although PL broadening can be attributed to impurities, lattice defects, alloying, or sample nonuniformity, it more likely results from compositional inhomogeneities which result from phase separation, as similarly observed for GaInAsP materials [30]. The gross broadening may result from carriers recombining in compositionally nonuniform, lower-energy-gap InSb-rich regions, which were detected in energy dispersive x-ray analysis in the scanning TEM [25]. Thus, the degradation of a periodic step structure as shown in Figure 2-6(c) is likely related to phase separation of the GaInAsSb.

$\rightarrow[\bar{1}10]$

(a)

(b)

(c)
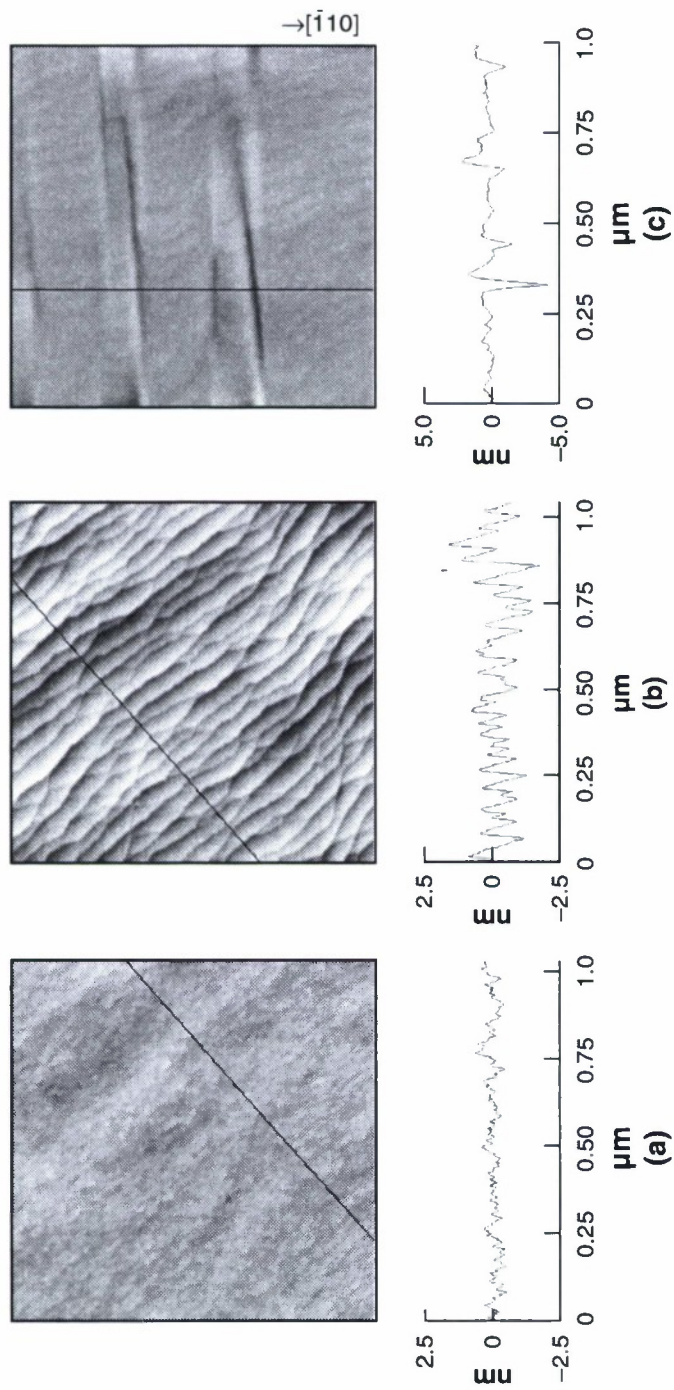
Figure 2-6. Atomic force microscope scans of $Ga_{1-x}In_xAs_ySb_{1-y}$ grown on (001) GaSb miscut 2° toward (101):
(a) growth temperature of 525°C and x = 0.16, y = 0.15; (b) growth temperature of 575°C and x = 0.12, y = 0.10;
(c) growth temperature of 575°C and x = 0.14, y = 0.12.
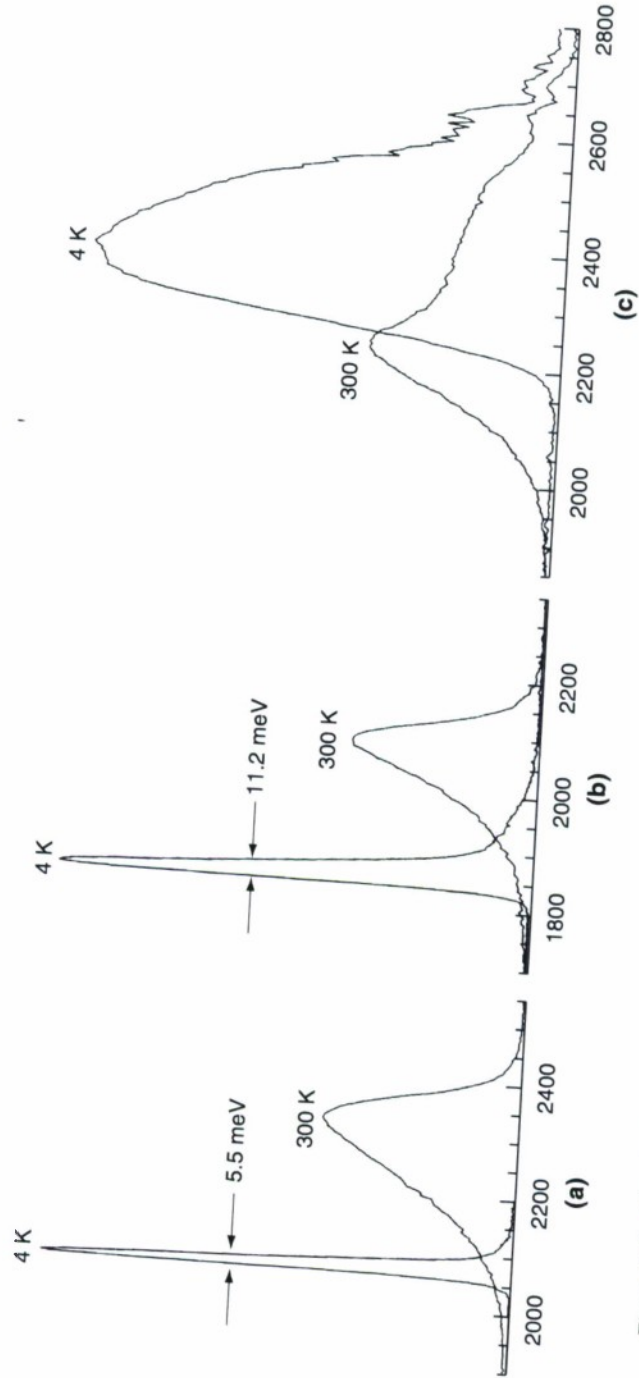
Figure 2-7. Photoluminescence spectra measured at 4 and 300 K of $Ga_{1-x}In_xAs_ySb_{1-y}$ shown in Figure 2-6: (a) growth temperature of 525°C and x = 0.16, y = 0.15; (b) growth temperature of 575°C and x = 0.12, y = 0.10; (c) growth temperature of 575°C and x = 0.14, y = 0.12.
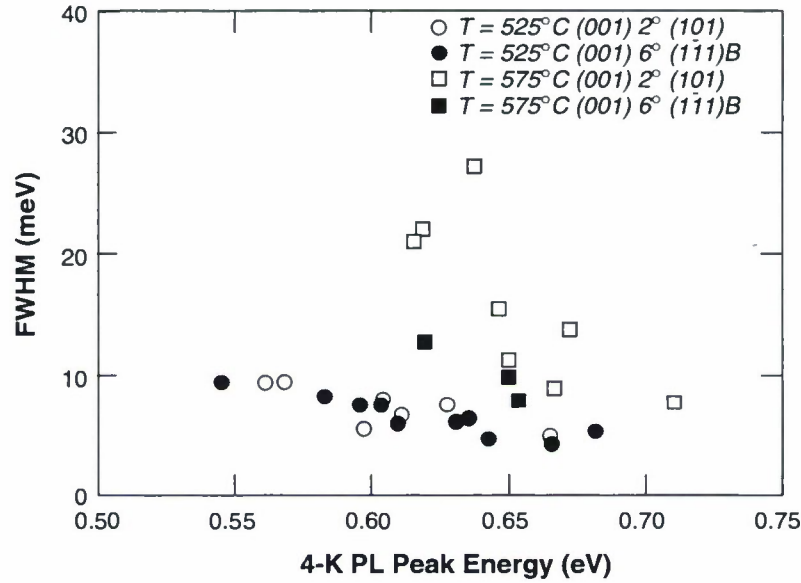
Figure 2-8. Photoluminescence full width at half-maximum (FWHM) measured at 4 K of GaInAsSb grown at 525 and 575°C on (001) *GaSb miscut 2° toward* (101) *or 6° toward* ($1\bar{1}1$) *B.*

The 4-K PL FWHM values can provide a semiquantitative measure of the degree of phase separation [30]. Figure 2-8 summarizes these values as a function the 4-K PL peak energy for GaInAsSb grown at 525 and 575°C on (001) GaSb miscut 2° toward (101) or 6° toward ($1\bar{1}1$) B. Only data with a blue-shifted 4-K PL peak energy with respect to the 300-K PL energy are included. Overall, the FWHM values increase with decreasing PL peak energy, which is in line with the fact that lower energy is associated with larger x- and y-values and an increased tendency to phase separate. The FWHM values are similar for layers grown at 525°C whether the miscut angle is 2 or 6°. However, at 575°C, these values are significantly larger and suggest a higher degree of phase-separated material. In addition, the FWHM values are larger for the epilayers grown on the 2° miscut substrates compared to the 6° miscut. AFM studies for these 6° samples indicated that the surface is vicinal at 525°C, and step bunched at 575°C. For the 6° step-bunched surface, the terrace lengths are shorter and the step heights are larger than for the 2° miscut substrates. The terrace lengths and step heights are about 28 and 2.6 nm, respectively, for the 6° miscut, compared to 39 and 1.5 nm, respectively, for the 2° miscut.

The surface step structure of GaInAsSb appears to have an important influence on the degree of phase separation. The AFM results suggest that GaInAsSb is deposited in a step-flow growth mode. If the adatoms are assumed to migrate freely on terraces until they become incorporated at steps or kinks, the

19
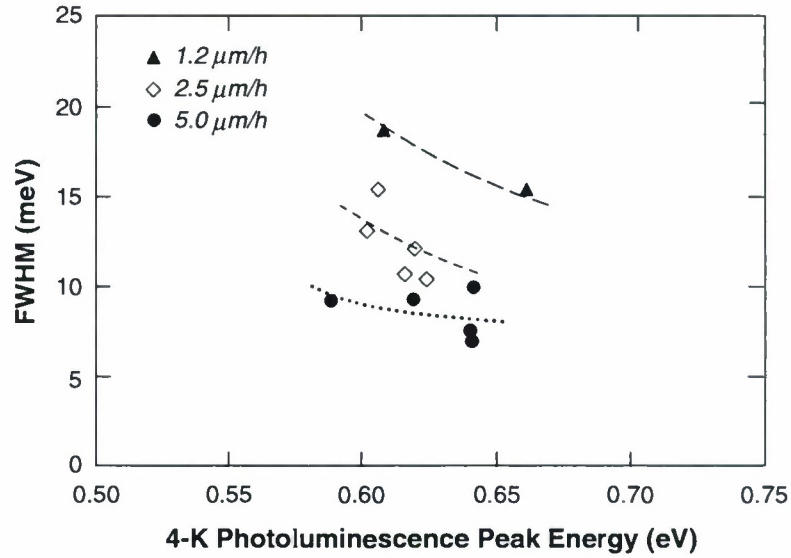
Figure 2-9. Photoluminescence FWHM measured at 4 K of GaInAsSb grown at 1.2 µm/h (triangles), 2.5 µm/h (diamonds), and 5 µm/h (circles).

longer terrace lengths of a step-bunched surface may provide more time for the system to approach thermodynamic equilibrium. The longer lifetimes promote alloy clustering, and thus the degree of phase separation increases. Therefore, vicinal surfaces at 525°C are preferable to step-bunched surfaces at 575°C. For layers grown at 575°C, the smaller 4-K PL FWHM values of the 6° miscut samples compared to the 2° miscut samples may be attributed to shorter terrace lengths and higher step heights of the 6° surface, which reduce the lifetime. Apparently at 525°C, the lower adatom diffusivity and the small terrace lengths (9 and 3 nm for the 2 and 6° miscut surfaces, respectively, not measured but geometrically inferred) greatly reduce the lifetime and limit the degree of phase separation.

If adatom lifetime is an important factor, then an increase in the adatom flux, which increases the growth rate, would decrease the lifetime. Figure 2-9 shows 4-K PL FWHM data for GaInAsSb grown at rates from 1.2 to 5 µm/h. The FWHM values decrease with increasing growth rate: the spectral width for ~0.6-eV peak energy decreases from ~18 meV at 1.2 µm/h to <10 meV at 5 µm/h.

Thus, a strong correlation exists between the surface step structure of GaInAsSb epilayers and the degree of phase separation, which is evaluated by PL. A periodic step structure is associated with good PL properties, while an irregular surface correlates with extremely broadened PL spectra. Vicinal surfaces are observed for growth at 525°C compared to step-bunched ones at 575°C, and the optical properties are significantly better for layers grown at the lower growth temperature. Although thermodynamics suggest

that the growth of these metastable alloys would be more stabilized at the higher growth temperature, our results show an opposite trend. The longer terraces on step-bunched surfaces may be associated with longer adatom lifetimes which increase the tendency for the GaInAsSb alloy to approach the thermodynamically favored phase-separated state.

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3. SUBMICROMETER TECHNOLOGY

3.1 HIGH-RESOLUTION STEREOLITHOGRAPHIC PATTERNING USING INTEGRATED-CIRCUIT-COMPATIBLE PHOTORESISTS

Stereolithographic patterning enables rapid prototyping of complicated three-dimensional structures. Parts are built up in a layer-by-layer manner with no tooling or mounting changes during the build operation, drastically reducing fabrication times. Components are also in many instances built directly from a three-dimensional computer representation. Until recently, most stereolithographic techniques concentrated on fabricating macroscopic components (i.e., >1 cm^3) with limited resolutions (i.e., >1 mil, or 25 μm). We have developed a technique that enables microscopic parts to be fabricated stereolithographically utilizing photoresist materials and spin-coating techniques used in the integrated circuit (IC) industry for high-resolution high-throughput lithography. Parts are patterned on a layer-by-layer basis using repetitive resist application and exposure techniques, followed by a single development step. With the use of investment casting techniques, parts can be replicated in a wide variety of materials. We believe this technology will benefit the design of high-performance miniaturized systems such as waveguide- and fluidic-based devices, enabling the fabrication of structures with optimized shapes and flow characteristics.

Photoresists used in IC fabrication comprise three basic elements: matrix resin, photoactive component, and solvent. The matrix resin provides the primary thin-film properties such as thermal stability and etch resistance of the photoresist. Exposure of the photoactive compound (PAC), or sensitizer, alters the solubility of the resin in a chemical developer. Solvents are chosen that readily dissolve the solid contents of the resist and have the appropriate evaporation rate and viscosity such that uniform thin films can be applied by spin casting. The key challenge with our stereolithography approach is preventing the coating solvent from intermixing with previously defined layers as each new resist layer is applied. Solvent penetration can cause a washing out of previously defined features as well as thickness nonuniformities after coating.

To enable multiple layers of resists to be successively applied and imaged, a new technique has been developed to prevent solvent intermixing between layers. The resist is first redissolved in a weaker, less polar solvent. A surface treatment is performed between each layer to increase the hydrophilicity at the surface, in effect repelling the less polar solvent in the newly applied layer. We have demonstrated this technique in Shipley 1813, a commercially available novolac-based G-line resist. The resist is normally dissolved in propylene glycol monomethyl ether acetate (PGMEA), a relatively polar solvent. We have found chlorobenzene, a relatively nonpolar solvent, can be used to alter the polar nature of the solvent while still retaining solubility. Chlorobenzene also has a relatively low evaporation rate, making it a good casting solvent for spin coating. To alter the hydrophilicity at the surface, we have used an ozone-based surface treatment. Previous studies have reported that exposing hydrocarbon-based polymers to ozone generates highly polar carbonyl (–C=O) and hydroxyl (–OH) end groups [1]. Contact angle studies can be
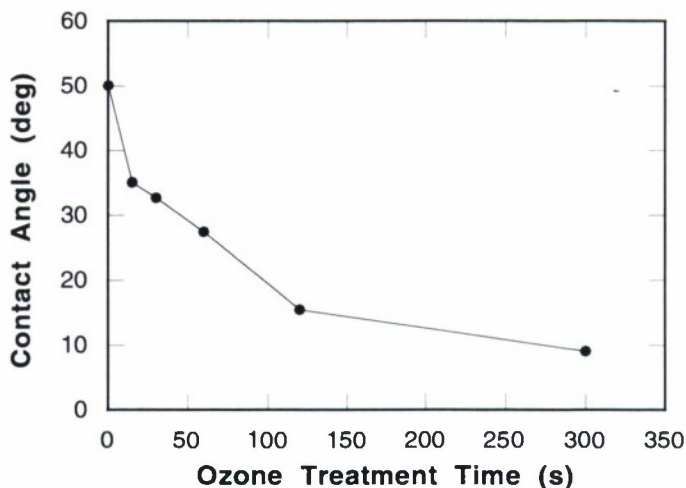
Figure 3-1.   Contact angle for dionized water droplets as a function of ozone treatment time. The ozone concentration is one-quarter percent in air. Wafers were coated with Shipley 1813 novolac-based photoresist and baked at 100°C for 1 min.

used to demonstrate these trends. Figure 3-1 shows the change in contact angle as a function of ozone treatment for 1-μL droplets of water placed on surfaces exposed to one-quarter percent ozone in air. The contact angle decreases substantially for highly polar water, indicating increased wettability of the surface. Measurements of contact angles for two different liquids can be used to quantify changes in the dispersive and polar contributions to surface energy [2]. Results of this analysis are shown in Figure 3-2, demonstrating that at modest concentrations of ozone the surface energy tends to saturate after ~2 min. Using an in-situ development rate monitor, we have experimentally confirmed that the ozone process only alters the surface and does not affect the bulk dissolution properties of the resist.

A simple procedure can be performed to calibrate the appropriate combination of solvent system and surface treatment time. A thin film of photoresist is spun on a silicon wafer. After the post-apply bake (PAB), the photoresist is exposed with a grating pattern. The photoresist surface is then treated with ozone for several different times. After ozone treatment, different co-solvent systems are spin coated over the photoresist surface. The remaining photoresist is developed, and surface profile measurements are made to determine the thickness and edge profile of the patterned lines. If solvent penetration has occurred, there will be a loss of resist thickness and feature definition in the patterned lines. Shown in Figure 3-3 are the results of spinning different ratios of PGMEA and chlorobenzene over patterned resist, demonstrating that the loss of resist thickness and feature definition can be prevented with the appropriate combination of ozone treatment and co-solvent system.

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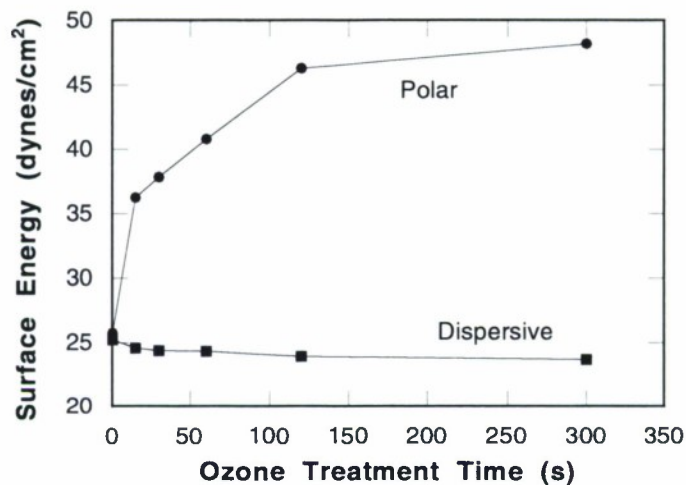
Figure 3-2. Polar and dispersive components of surface energy as a function of ozone treatment time using the experimental conditions in Figure 3-1.
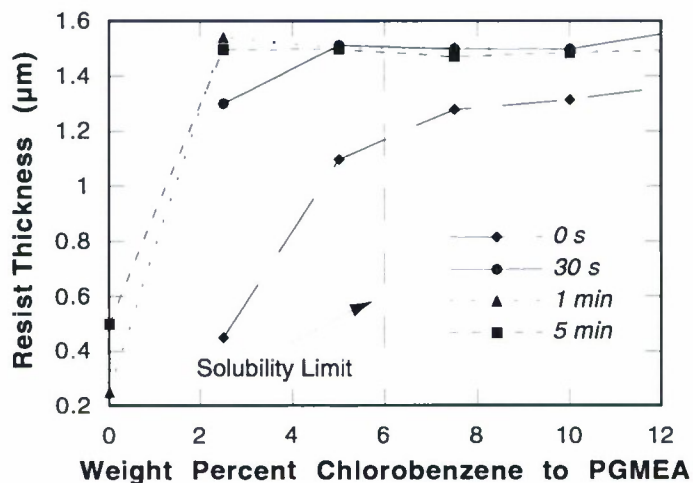
Figure 3-3. Optimization of co-solvent ratio and ozone treatment time to prevent resist intermixing effects. The measured film thickness is illustrated for a patterned 1.5-μm layer of photoresist after exposure to various co-solvent mixtures of chlorobenzene and propylene glycol monomethyl ether acetate (PGMEA). In these experiments, the co-solvent system was applied to the photoresist surface and then spin coated to promote evaporation. Note the solid content of the resist is found to precipitate out of solution at chlorobenzene-to-PGMEA ratios exceeding 6:1.

25

We have implemented a simple exposure tool using a scanning laser beam to demonstrate five-layer structures. The laser source is an 8-mW continuous-wave HeCd laser operating at 325-nm wavelength. The exposure tool provides controlled dose over selected regions and overlay capabilities for accurate alignment between layers. To pattern multilayer structures, the basic process flow is similar to the technique used in IC patterning and is summarized schematically in Figure 3-4. A layer of Shipley 1813 photoresist reformulated in four parts chlorobenzene to one part PGMEA is applied in a uniform thin film. After coating, a 1-min 100°C PAB is performed to drive out the coating solvent. A scanned laser beam patterns the resist in slices cut from a three-dimensional computer-aided design (CAD) drawing of the component. After exposure, the surface is exposed to ozone for 1 min. The process is repeated layer by layer until patterning is complete. The latent image is then developed in 0.175-N KOH developer. We have measured optical parameters and dissolution rates of the resist that enable accurate prediction of the resulting resist profiles, following the procedure first presented by Dill et al. [3]. We have extended the analysis to account for light penetration into underlayers, which increases the level of solubility. Shown in Figure 3-5 are the predicted doses necessary to pattern a staircase in five 1.5-μm-thick layers of photoresist, and the simulated depth profiles during development. The development rate of photoresist increases with increasing exposure dose. Thus, to reduce total development times, higher doses are used over exposed areas of the previous layer. In this manner, development proceeds more rapidly over interior portions of the structure. Shown in Figure 3-6 is the experimentally measured average step height of the staircase pattern. A slight offset occurs on the first step, but otherwise the incremental spacing between steps is within the experimental errors of our setup. Figure 3-7 shows a practical demonstration of this stereolithography technique; a microfluidic component was fabricated in five layers of 1813 photoresist.

The multilayer patterning process that has been developed is, we believe, rather general and can be tailored to both positive- and negative-tone resists over a broad range of exposure wavelengths ranging from near to vacuum uv. The technique leverages the incredible investment in resist development and processing equipment that has occurred over the last 30 years. Although this technique is targeted toward applications requiring thousands of layers, the technique we outline for preventing solvent intermixing may have useful applications in high-resolution patterning of semiconductor devices, particularly in mixing optical with e-beam or x-ray exposures on the same mask level.

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Resist: Resin + PAC + Solvent

Spin Coat
Bake (PAB)

Expose

O_3 O_3 O_3 O_3 O_3 O_3 O_3

Surface Treatment

Continue Layering Until Structure Defined

Bake (PEB)
Optional

Develop
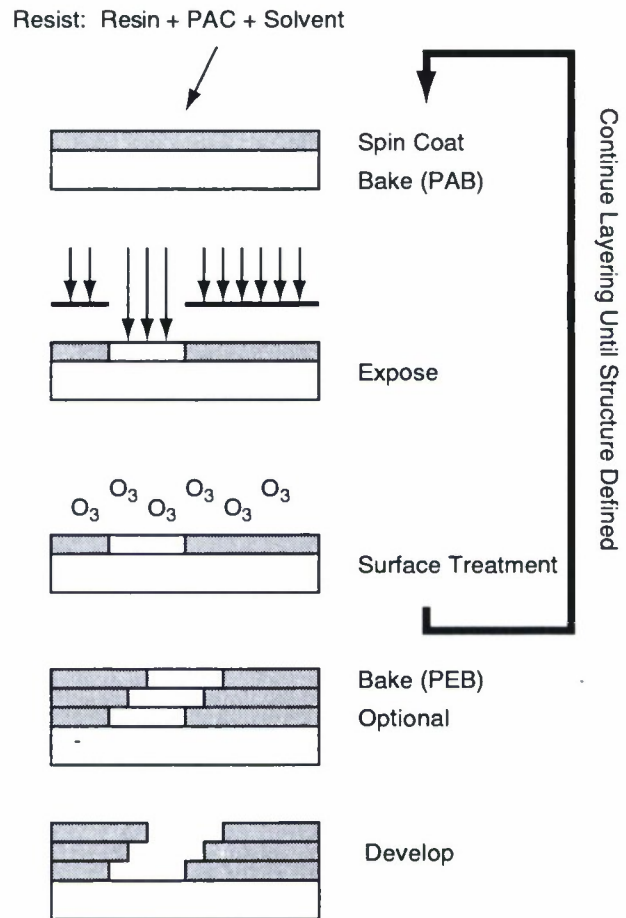
Figure 3-4. Process flow for multilayer patterning.

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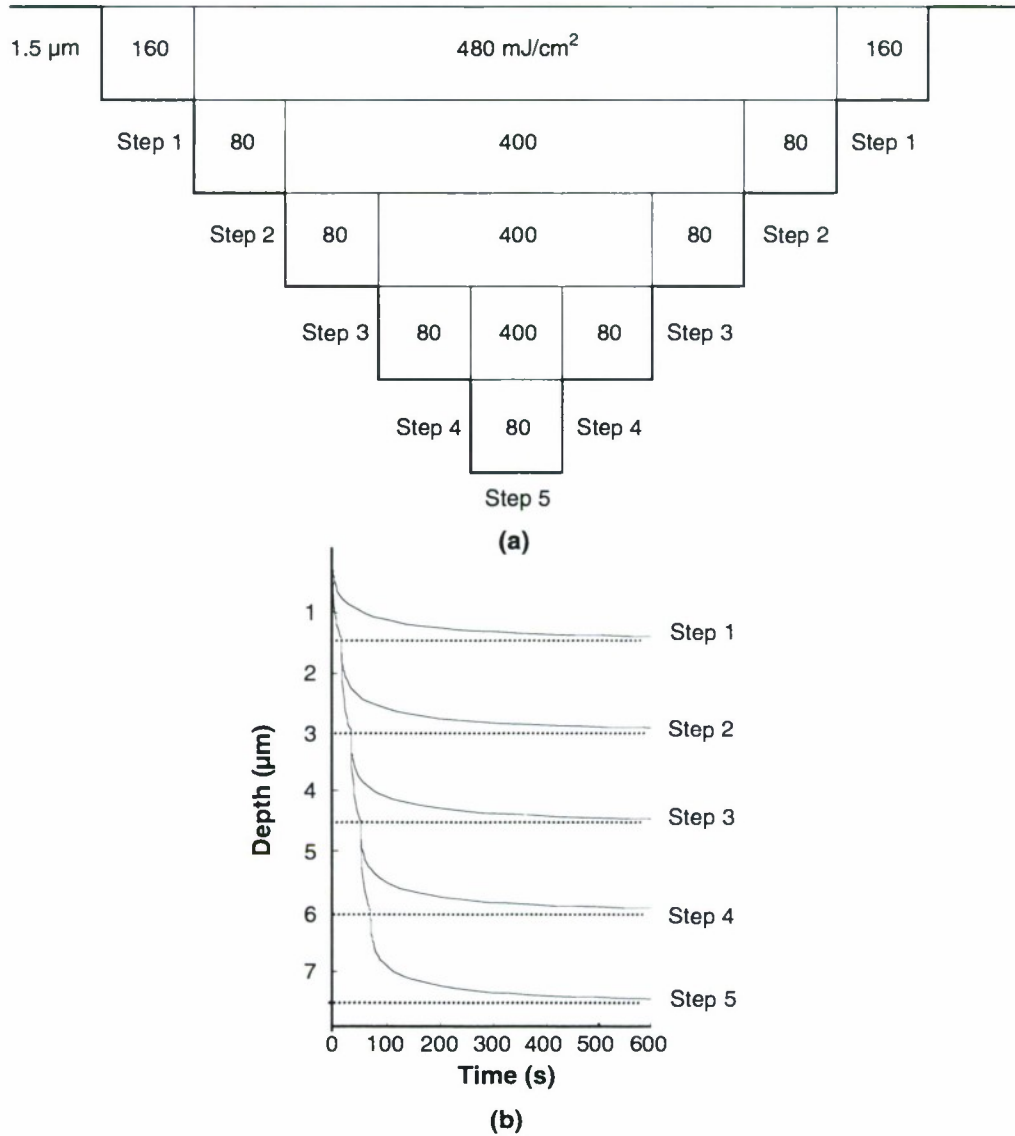
Figure 3-5. (a) Exposure doses in mJ/cm² used to pattern a five-step staircase structure in 1.5-μm-thick layers. The doses compensate for light leakage between layers. Higher doses are used over interior portions of the structure to promote dissolution. Using a uniform dose over the entire structure would limit the exposure energy to the value used to terminate at the bottom of the level (i.e., the dose used over step 1). Development would proceed rapidly at the beginning of a layer but quickly decelerate near the bottom of the level. In a multilayer application this could easily increase development times by orders of magnitude. (b) Predicted resist loss as a function of time over the different steps, showing the improvement in development time that occurs using dose modulation.

28
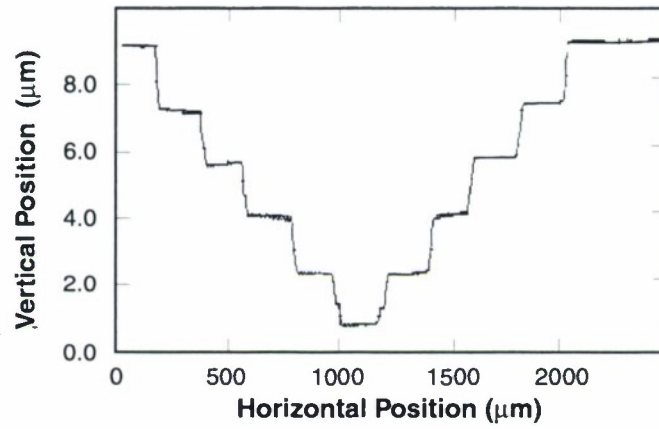
(a)
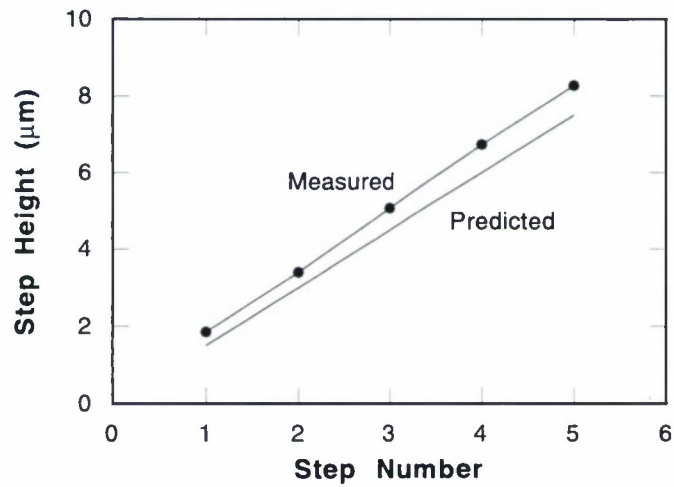
(b)

Figure 3-6. (a) Surface profile measurement of a staircase structure using the doses described in Figure 3-5. (b) Graph of average step height, showing that a slight offset of 0.2 μm occurs at the first layer and that the incremental spacing between layers is 1.62 μm.

250 µm
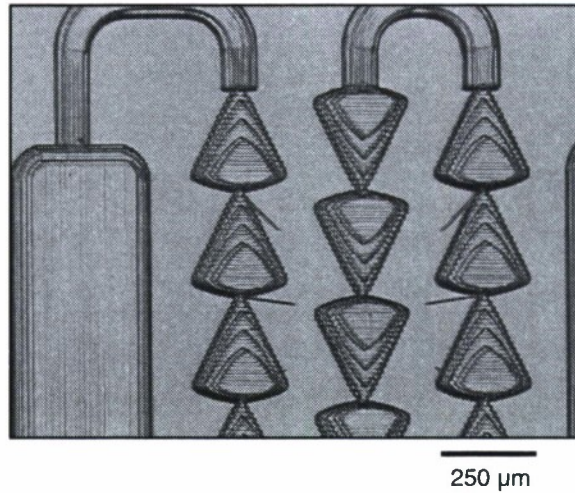
Figure 3-7. Optical micrograph of a five-layer microfluidic component structure. The stray lines and coarse edges are artifacts of the laser scanning exposure system.

3.2 INTEGRATED 1.55-µm OPTICAL STRUCTURES IN SILICON

Channel-dropping filters are a key component for wavelength-division-multiplexing (WDM) signal transmission systems. The purpose of these filters is to select an individual signal wavelength from the spectrum transmitted down the fiber. Filters are realized using fiber-Bragg gratings or normal transmission through thin film stacks on transparent substrates. Both types of devices are complex to manufacture and combine in a system. Planar thin film resonator structures have been proposed to perform the channel selection function. The micro-ring resonator, shown in Figure 3-8, has been extensively analyzed and demonstrated in several materials [4]–[6]. These structures have the potential to be fabricated using conventional silicon microelectronics processing methods, which would result in very inexpensive WDM components [7].

Previously, micro-ring resonators fabricated using optical lithography suffered from poor pattern fidelity, resulting in low Q's [5]. This limits the filter's ability to discriminate a single wavelength from adjacent channels. High-Q micro-ring resonators have been fabricated in III-V compounds using e-beam lithography [6], but the long writing times limit the overall process throughput, increasing the manufacturing cost of the component. The ability to fabricate these structures in silicon using optical lithography is a key requirement in realizing the tremendous cost saving of conventional IC techniques.

30

The factors determining the Q are the loss mechanisms from the micro-ring resonator. Loss of optical energy arises from the coupling of light out of the ring at the input and output guides, scattering losses in the rings themselves, and internal losses in the ring materials [4]. Previously, it has been demonstrated that thin film polycrystalline silicon, with proper annealing, can be used for low-loss waveguides [8],[9]. The main limitation to date has been the definition and etching of the ring pattern, in particular, the gaps between the ring and input and output guides. When the gaps are closed, modeling has shown that the light tends to radiate out from the gap region into free space and is lost [5].

In the present effort, micro-ring resonators have been fabricated in polycrystalline silicon (poly-Si). Particular attention has been paid to the 248-nm optical lithography process and the etching process in order to obtain subwavelength-resolution coupling gaps [10]. A 2.0-μm-thick thermal oxide is grown in order to reduce substrate losses due to poor confinement. The waveguide film is deposited on top of the thermal oxide buffer. The required thickness (200 nm) depends on the design requirements for single-mode confinement at a wavelength of 1.55 μm. Amorphous silicon, deposited in a CVD process, has high losses at 1.55 μm, and is converted to poly-Si using an oxide-capped annealing process, which results in relatively smooth surfaces required for low scattering losses [9]. After annealing, the capping oxide is stripped, and the poly-Si film is patterned. The resist/antireflective coating stack was optimized using modeling techniques to maximize the resolution. On the reticle, micro-ring resonator structures with several gaps were available for process optimization. By using a dose focus array, conditions were determined for printing 0.1-μm gaps using a 0.15-μm feature size with a dark-field mask and Shipley CGR (negative tone) resist. These conditions were then used to expose all fields of an entire 6-in. wafer. Similar resolution results were obtained over a 12-wafer lot. These patterns were subsequently transferred into the poly-Si film using a fluorocarbon plasma-etching process. A cross section of the waveguide is shown in Figure 3-9. Figure 3-10 demonstrates the ability of the overall process to define very narrow gaps (<0.1 μm). These dimensions represent subwavelength resolution for the 248-nm wavelength of the optical stepper.

The performance of the micro-ring resonators has been measured in the 1.55-μm fiber communications band. Light from a tunable laser is focused from a fiber pigtail onto the polished input facet of the micro-ring resonator. Output light is collected using a lock-in technique to improve the signal-to-noise ratio. The transmission spectrum of the channel drop and through ports is shown in Figure 3-11. The measured Q is on the order of 2000, and represents the best performance reported to date for a poly-Si micro-ring resonator. The free-spectral range is 22.7 nm. Another key result is the large fractional power extraction at the resonant wavelength. Complete power extraction is a key characteristic of micro-ring resonators owing to the matching of the through and drop port coupling regions.

31

Previous results for optically printed poly-Si micro-ring resonators exhibited a Q of 120. Further improvements in guide cross section and reductions in sidewall roughness will result in higher Q's. The theoretical limit is 10 000 for these structures.

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M. Fritze   B. Little*
S. C. Palmateer   L. C. Kimerling*
D. K. Astolfi   H. A. Haus
S. G. Cann
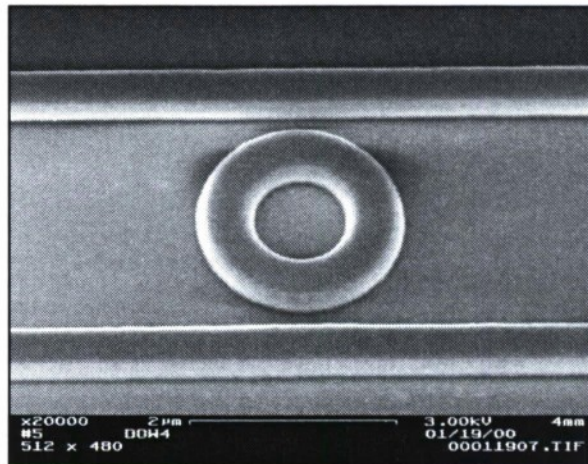
Figure 3-8. Scanning electron micrograph (SEM) of a 2-µm-diam micro-ring resonator structure fabricated in a 200-nm-thick poly-Si film, at a viewing angle of 45° from vertical. The ring resonator is simultaneously coupled to two straight guides, which function as input and output ports. At the resonant wavelength, light is efficiently coupled (up to 100%) through the ring into the alternate guide, which can function as the channel drop port in a wavelength-division-multiplexing system. Off resonance, the light transmits past the ring, providing a through port for the nonresonant wavelengths.

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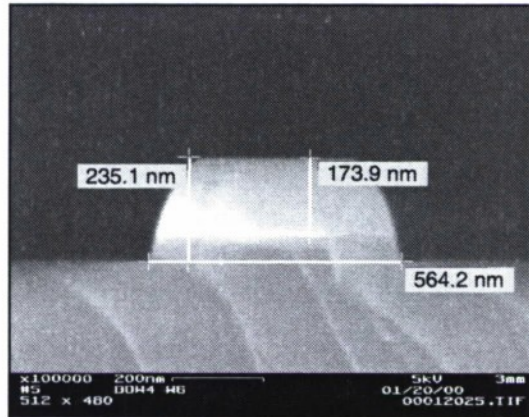
Figure 3-9. SEM cross section of a poly-Si waveguide designed for single-mode operation at 1.55 μm. The bright part of the guide is the poly-Si while the darker material below is the thermal oxide buffer. The texturing of the guide and 2-μm buffer are indicative of the poor cleaving characteristics of the film stack, and hence facet polishing is required to reduce input-output facet losses. Rounded shoulders of the guide are due to resist mask erosion during the etching process, an undesirable feature that contributes to sidewall roughness and optical scattering losses.
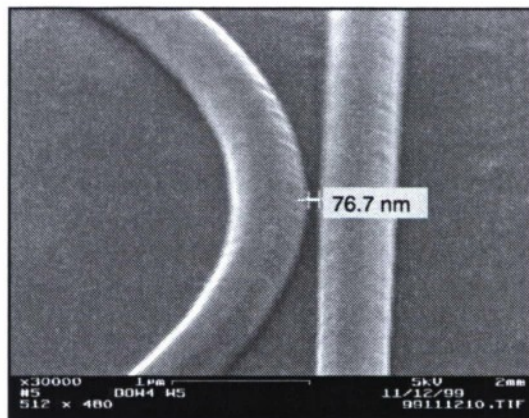
Figure 3-10. SEM of the coupling gap between a straight guide and a 5-μm-diam ring, at a viewing angle of 45°. The coupling gap of 77 nm is subresolution for the 248-nm-wavelength optical stepper, but was achieved using process enhancements outlined above and in [10]. Narrow coupling gaps are required for high-index materials, such as poly-Si, where the optical wave is tightly confined to the guide. As discussed in Figure 3-9, the roughness on the shoulders of the guide can be a source of optical scattering, and hence loss, depending on its length scale.
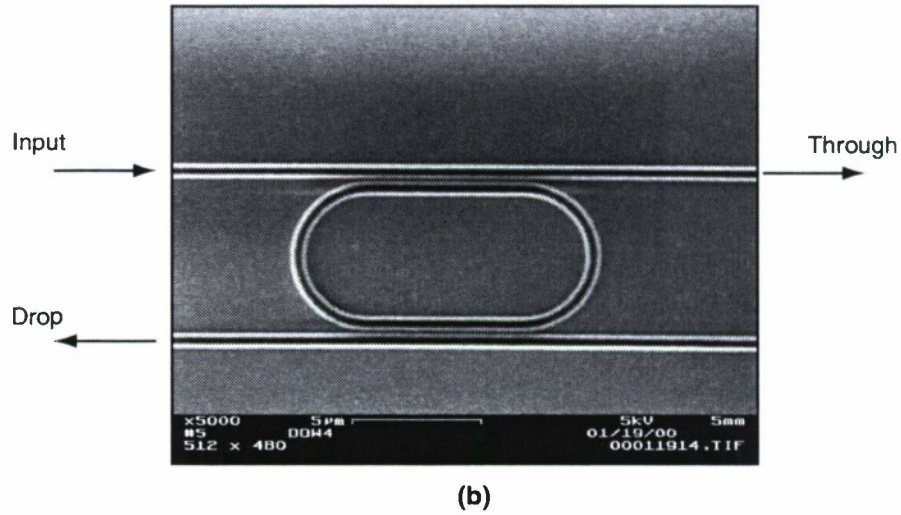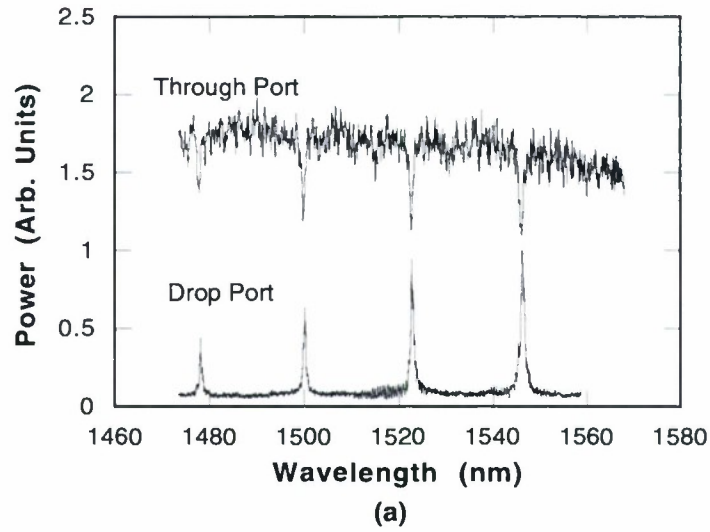
Figure 3-11. (a) *Spectral transmission of a racetrack micro-ring resonator implementing a channel drop filter in the 1.55-μm fiber communications band. The upper spectrum displays the through port transmission characteristic, with the evident power extraction at the resonant wavelengths. The lower spectrum displays the drop port characteristic, with the corresponding peaks in the transmission characteristic as power is efficiently extracted at the resonant wavelength. The resonator Q is calculated from the resonant wavelength divided by the full width at half-maximum spectral width of the drop channel at resonance. At a Q of 2000, these racetrack resonators are the best reported for poly-Si. The periodic spectral separation of the resonant drop wavelengths (22.7 nm) is termed the free spectral range (FSR) and is a function of the ring circumference and the effective group velocity. Very small diameter ring resonators, such as shown in Figure 3-8, have a measured FSR >100 nm. The noise in the through transmission spectrum is due to Fabry-Perot resonances between input and output facets of the through port.* (b) *SEM of a racetrack resonator, indicating the input, through, and drop ports. The coupling gap is 144 nm.*

34

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4. BIOSENSOR AND MOLECULAR TECHNOLOGIES

4.1 FORMATION OF BILAYER LIPID MEMBRANES FOR ARTIFICIAL CELLS

For over a billion years, living cells have been sensing and interacting with their environment via protein receptors and ion channels on the cell membrane surface. These binding and signaling reactions happen in <1 s, and offer major advantages for rapid biological and chemical sensing with high sensitivity (down to single-molecule/antigen levels). Many other complex and useful bioelectrochemical processes happen inside the cell as well, which may someday enable other kinds of applications such as programmable intracellular biochemical manufacturing or biocomputing.

An artificial "cell-on-a-chip," in which key "components" from the cell are reproduced in a more robust framework, could provide the enabling technology base for new classes of biological and chemical detectors and other biodevices. In the detectors the sensitive, fast-acting sensors that nature has already engineered on cell membranes could be linked directly to silicon circuits without the need for maintaining a full living system. Such a cell-silicon system can be a nonliving analog to a cell-based biosensor, and furthermore can exploit the considerable signal processing capabilities currently available in silicon. In addition, for basic science, the ability to generate an array of nonliving "cells" in a controlled fashion on a chip provides a platform for the study of the fundamental structure and function of cellular and membrane-bound proteins.

The two technologies required for the realization of an artificial cell on a chip that uses these membrane-bound receptors are the development of regenerable artificial cell membranes using lipid bilayers, and the ability to make and insert protein receptor complexes into such membranes in situ.

The cell membrane is composed primarily of lipid molecules arranged in a bilayer, and is therefore referred to as a bilayer lipid membrane (BLM). This report provides an overview of the physics of formation of a BLM. Currently available literature detailing the mechanics of the BLM formation process indicates that they form spontaneously under suitable initiation conditions, and analytical solutions are available and can be used to predict the stability of certain lipid systems for a given physical support geometry, or conversely to design appropriate supports. As an answer to the first requirement for artificial cells on chips, we have performed an analysis, using models from the literature, to determine whether or not BLMs may be stably formed on micromachined substrates. We can then use these results to develop a microfabricated silicon-based device that will be capable of generating artificial BLMs. This device will be able to monitor and regenerate the membrane, thereby addressing the important issues of lifetime and reliability of a sensor using the BLM. Once stable BLMs can be formed in arrays in a reproducible manner, they can serve as a platform for the study of the artificial receptor complexes referred to in the second requirement.

The BLM is composed of closely packed lipid molecules that self-assemble into a bilayer, with outer hydrophilic polar headgroups and inward-facing hydrophobic tails. When formed on an aperture, the BLM
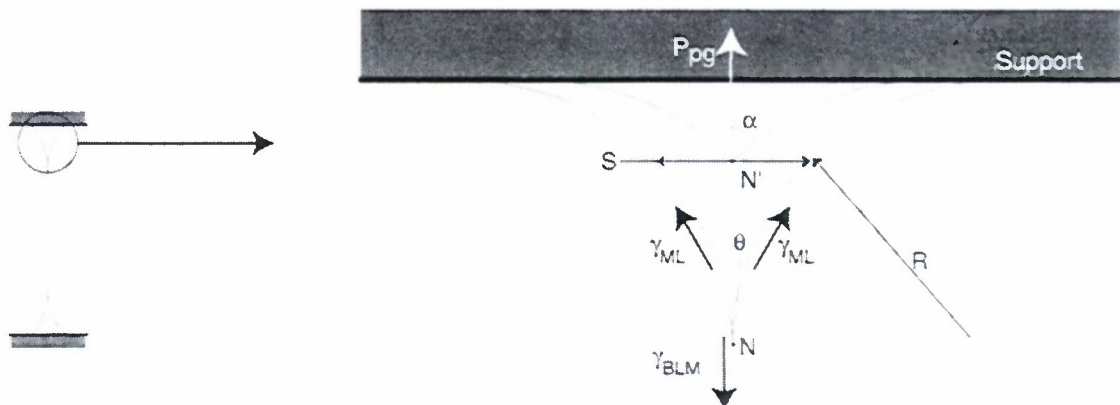
Figure 4-1. Bilayer lipid membrane and details of Plateau-Gibbs (PG) border region geometry. The bilayer interfacial tension $\gamma_{BLM} = 2\gamma_{ML}\cos\alpha + P_{pg}$, where the PG border suction pressure $P_{pg} = S\gamma_{ML}/R$. $S = 2R(\cos\theta - \cos\alpha)$, where S is the change in PG border width as the bilayer periphery expands from N to N'.

takes the form shown in Figure 4-1, where the membrane has two distinct regions—a thin bilayer and a thick Plateau-Gibbs (PG) border region. Normally, BLMs are formed by introducing a droplet of material into the aperture, which is immersed in a salt solution. Depending on the forces exerted on the droplet (as well as the surface conditions of the support aperture), it will thin spontaneously to the bilayer + border state, remain as a globule, or drain partially to form a thicker multilayer + border structure. Thinning consists of drainage of the excess lipid material into the PG border and then the support, due to hydrostatic pressures and interfacial tensions on both sides of the BLM. If attractive (PG border suction, van der Waals attraction between lipid molecules) and repulsive (Born repulsion between polar headgroups) forces balance, then the membrane will remain in a stable state.

The interfacial surface tension of the membrane (γ_{ML} for monolayers and γ_{BLM} for bilayers) is a key parameter of a BLM, and is defined as the work required to create a new unit area of lipid layer. From Figure 4-1, at equilibrium, there is a balance between the BLM and the PG border bulk material. γ_{BLM} is balanced by the interfacial tensions of the monolayers on the PG border, and the PG border suction pressure P_{pg}. For a non-zero contact angle θ between the BLM and the PG border, the border will move towards the support, from N to N'. In a simple analysis [1], assuming that the PG border boundary takes a spherical shape, basic geometrical considerations result in the model for the BLM and PG border, as shown in Figure 4-1. Therefore $\gamma_{BLM} = 2\gamma_{ML}\cos\theta$. If $\theta = 0$ then the membrane will not thin and no bilayer will form. If $\theta > 0$ then $\gamma_{BLM} < 2\gamma_{ML}$ and the PG border will move towards the support rim until equilibrium has been reached, at which time $\theta = \alpha$ and P_{pg} will equal zero.

A more detailed analysis is given in [2], in which the shape of the toroidal annulus making up the PG border is determined using variational calculus. In this case, the shape is determined by minimizing the surface area of the PG border annulus given a fixed volume of lipid material, with boundary conditions obtained from the equilibrium conditions shown above ($\gamma_{BLM} = 2\gamma_{ML}\cos\theta$ and $\gamma_{SW} = \gamma_{SB} + \gamma_{ML}\cos\beta$, where γ_{SW} = tension at support-water interface and γ_{SB} = tension at support-border interface). The solutions are obtained assuming no buoyant forces and take the form of elliptic integrals. They can be used to determine support geometries required to maximize BLM diameter.

The dynamics of BLMs were investigated in [3], using an extension of the above model. It was found that the dynamics of thinning is influenced by the geometry of the support, which affects the border suction pressure. A spring-dashpot linear dynamic model of the border was presented as a means of extracting the frequency response of the membrane and PG border as it is subjected to time-varying stretching pressures.

All of the above solutions require numerical estimates of the interfacial tensions between various components of the system. A standard method for evaluating the interfacial tension is the maximum bubble pressure technique, which can be used with the Laplace-Young equation ($P_{hp} = 2\gamma/R_c$ for a spherical bubble with radius of curvature R_c; P_{hp} is the hydrostatic pressure on the film) to experimentally determine γ. For typical BLM lipids, γ_{BLM} has a measured range of 0.1–5 dyne/cm.

The elastic moduli of a BLM have been derived to be $\kappa_s = \gamma$, and $\kappa_Y = \gamma/\delta_h$, where κ_s is the surface modulus, κ_Y is the Young's modulus, and δ_h is the membrane thickness. Therefore, measurements of these moduli also provide values for interface tensions. Some experimentally determined values from capacitance, resistivity, and interferometric measurements are provided in [4].

The ability of a BLM to form can also be evaluated in terms of free energies [1]. A BLM is a composite of two interfaces making up a water/oil/water (w/o/w) system. BLM formation is thought to have three stages, driven by the reduction of the free energy at the w/o/w interfaces. In the first stage a w/o/w interface is formed by introducing lipid material into the aperture in solution. In the second stage a thin lipid membrane forms in equilibrium with the PG border, due to migration of surface-active lipid molecules moving towards the w/o/w interface. This second stage is driven by diffusion and PG border suction, as well as any hydrostatic pressure differential across the membrane. Note that externally applied transmembrane potentials can also thin the membrane, through electrocompression effects ($P_{ec} = V^2[\varepsilon\varepsilon_0/2\delta_h^2]$, where P_{ec} = electrocompressive pressure, δ_h = BLM thickness, and V = transmembrane voltage [4]). The third stage is thought to start with a chance contact of oriented monolayers at the opposite w/o/w interfaces through thermal motion, mechanical vibration, or other local variations. This initiates a "zipper" action in which the rest of the membrane rapidly thins to the bilayer state owing to van der Waals attraction between molecules adjacent to the contacting ones. Simplistically, the following equations summarize the energy states of the three stages:

Lipid (o) + H$_2$O (w) $\rightarrow$ w/o/w biface + lipid + ΔF_1, where $\Delta F_1 = \gamma_{o/s} + \gamma_{o/w} - \gamma_{w/s} \cong 0$

w/o/w biface + lipid $\rightarrow$ monolayer + PG border + ΔF_2, where $\Delta F_2 = \gamma_{ML} - \gamma_{o/w}$

Monolayer + PG border $\rightarrow$ BLM + ΔF_3, where $\Delta F_3 = \gamma_{BLM} - \gamma_{ML}$

Net reaction: w/o/w biface + lipid $\rightarrow$ BLM + ΔF_i, where $\Delta F_i = \Delta F_2 + \Delta F_3 = \gamma_{BLM} - \gamma_{o/w}$

where o/s = oil/solid support, o/w = oil/water, and w/s = water/solid support.

Experimental data from a lecithin BLM give indicative numbers for the various quantities, and indicate that the overall free energy change is negative, since the BLM is the lowest free energy state of the system. Experimental evidence indicates that for $|\Delta F_i| < 40$ dyne/cm, the membrane will usually not spontaneously thin into a bilayer. Free energies of formation for various types of lipids, derived from contact angle measurements, are given in [5], and are shown to match fairly well to those calculated with the Hamaker-Lifshitz theory, which provides expressions for the forces and free energies between two sections of material A separated by material B where the interface interactions are primarily van der Waals forces.

An analysis and experimental study of a related structure, the spherical lipid membrane, is given in [6] in which the spheres are formed by large hydrostatic pressure differentials across the BLM; the resulting structure is basically identical to a soap bubble. In this case, Hamaker-Lifshitz theory is again used to calculate free energies of formation. This is an interesting structure to study in that an alternative approach to BLM generation is to create a lipid sphere and subsequently excise a portion of it to form the BLM, by attaching the sphere to the support aperture and removing the excess material.

Cell bilayer lipid membranes in plants and animals are predominantly composed of two lipid types—phosphatidyl choline (commonly known as lecithin) and phosphatidyl ethanolamine. Both molecules consist of a polar headgroup containing glycerol, a phosphate group, and a nitrogen-containing molecule (choline or ethanolamine), and two fatty acid tails (saturated $CH_3(CH_2)_n COOH$ or unsaturated $CH_3(CH_2)_x CH = CH(CH_2)_y COOH$, where $n = x + y = 14$ to 18). Cholesterol ($C_{27}H_{46}O$) is another vital component of animal cell membranes, providing rigidity to the membrane by filling the spaces between fatty acid chains.

Table 4-1 gives representative interfacial tensions and free energies for three lipid-solvent-aqueous solution systems commonly used to synthesize lipid membranes. Using the free energy criteria for formation described above, we see that in all cases $|\Delta F_i| > 40$, indicating that the BLM is expected to form spontaneously.

Experimentally determined interfacial tensions for typical lipid solutions as listed above and in the references indicate that it is possible to form stable BLMs, as long as the support rim is correctly designed

TABLE 4-1

**Representative Interfacial Tensions and Free Energies
for Three Lipid-Solvent-Aqueous Solution Systems**

Lipid/Solvent/Aqueous Solution	γ_{BLM} (dyne/cm)	γ_{ML} (dyne/cm)	ΔF_i (dyne/cm)
Lecithin (n = 18)/n-dodecane/water	0.9	6.5	−49
Bacterial phosphatidyl ethanolamine (n_{avg} = 16.6)/n-decane/0.1-M NaCl	7.8	3.9	−42
Cholesterol/n-octane/water	1.9	N/A	−48

and the aperture is sized to form a stable membrane (using an analysis similar to that in [2]). Selection of a suitable lipid/solvent/aqueous solution system (such as those listed above) ensures that the BLM will spontaneously form. We can take the commonly used bacterial phosphatidyl ethanolamine/n-decane system as an example of the support geometries required for forming a stable membrane. If we desire a BLM with a radius of 800 μm in an aperture of 1-mm radius, this can be achieved with a minimum support rim thickness of 250 μm. A thinner support would result in drainage of excess lipid material over the edge of the support, which may result in rupture of the membrane. However, such a structure is easily achievable with conventional micromachining and microfabrication techniques, and can be made in a simple fashion by laminating layers of silicon/glass/plastic to form channels.

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5. ADVANCED IMAGING TECHNOLOGY

5.1 OPERATION OF HIGHLY STRAINED, BACK-ILLUMINATED CCDS

As reported previously, the technique for thinning and operating back-illuminated charge-coupled devices (CCD) has been established [1]. The thinning technology has been used to fabricate thin silicon membranes, ~15 mm thick, which were then deformed [2]. This report details the effects of operating thinned and deformed CCDs.

The central region of CCDs was thinned from the back side to a thickness of ~15 μm, with a diameter of 10 μm, as shown in Figure 5-1. An individual CCD was then mounted in a pressure fixture that allowed the thinned section to be clamped between two O-rings, as seen in Figure 5-2, while electrical probes contacted the front side of the CCD. The CCD was lowered to temperatures in the vicinity of −50°C, and pressurized He gas was introduced into the fixture, impinging on the thinned back side of the device.
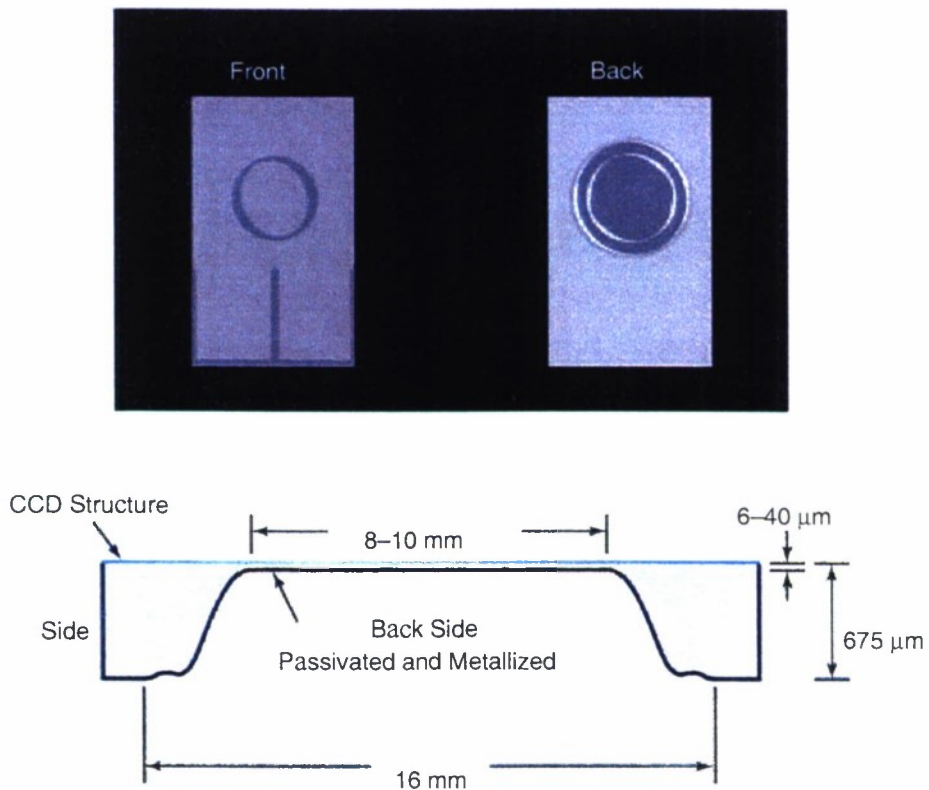
Figure 5-1. Thinned charge-coupled device geometry.
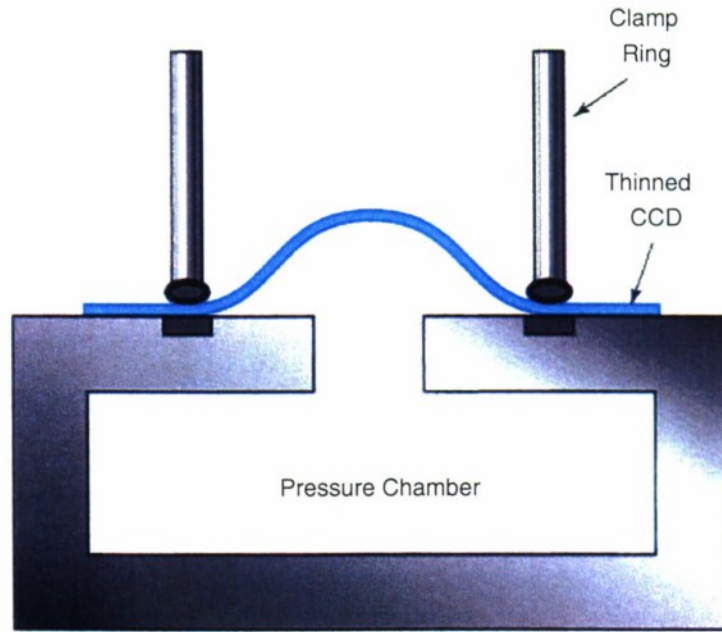
Figure 5-2. Test jig.

As the pressure was increased, the thinned section of the CCD was deformed upward, introducing a strain approaching 1.3% in tension in both the radial and tangential directions in the membrane [3]. The membrane would fail at higher strains, but the deflection and strain were reproducible at lower He pressure, indicating the deformation was elastic. Measurement of the dark current of the CCD vs gas pressure indicated a roughly exponential dependence on pressure, as shown in Figure 5-3; this behavior was also seen to be reproducible, even after deforming and relaxing the CCD several times. By altering both the pressure and temperature of operation of a number of CCDs, an analytical expression, which described the dark current very well, was described. This expression was $\ln(I_d) = \ln(I_0) - (E_g - dE_g/d\varepsilon \cdot \Delta\varepsilon)/kT$, where I_0 is a fitting constant, E_g is the energy gap of Si, $dE_g/d\varepsilon$ is the deformation potential of Si, and ε is the applied hydrostatic strain [4]. The value of $dE_g/d\varepsilon$ inferred from this work is 80 meV/(% strain), fairly close to the theoretical values of 115 meV/(% strain). This agreement is quite satisfactory, since the analytical model applied above [3] for strain state is itself an approximation.

The dependence of dark current vs position was also measured across the thinned region of the device and the results plotted in Figure 5-4. The dark current rises in the thinned section of the CCD, with the increase roughly following that predicted by the analytical model for strain in the membrane (the model predicts a cusp at the center of the thinned section, but this is not the case experimentally). The

44

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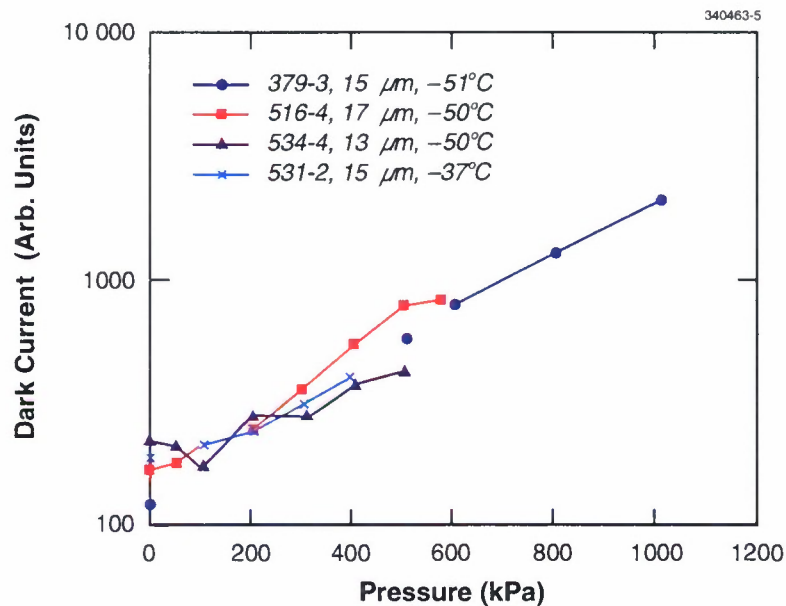
Figure 5-3. Dependence of dark current on pressure.

local maxima and minima seen in Figure 5-4 occur at the edge of the thinned region, where the CCD thickness changes from 15 to 525 μm. A good model to explain the strain state variation in this region does not exist.

Other measures of CCD performance, such as charge-transfer efficiency and noise, were not measured explicitly, but there did not appear to be any qualitative change in these quantities. In the thinned region, decreasing the temperature by at most 5°C reduced the dark current by a factor of 2, back to the unstrained values.

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V. S. Dolat
A. H. Loomis

575 kPa, −50°C
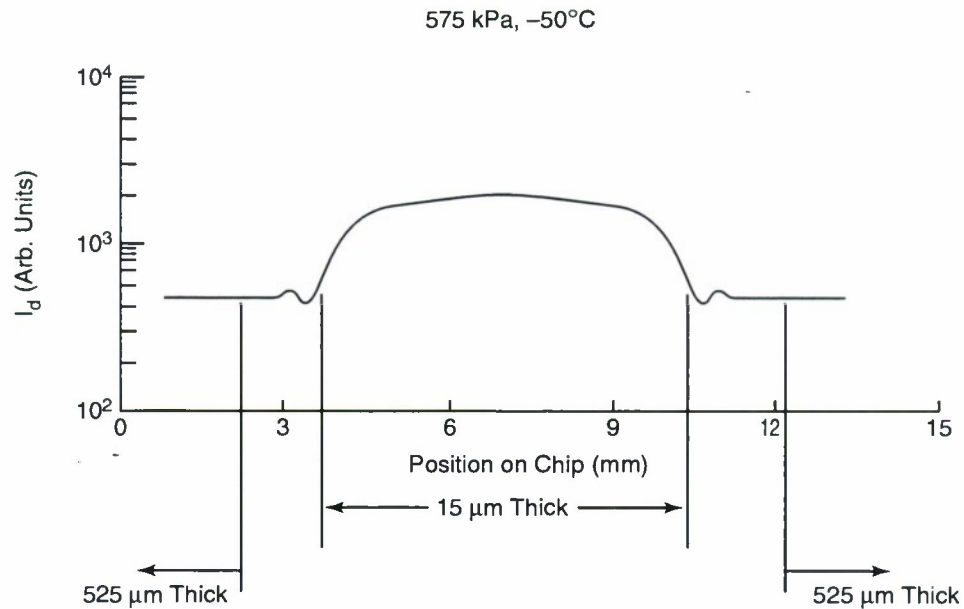
Figure 5-4. *I_d scan across center of thinned image array.*

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6. ANALOG DEVICE TECHNOLOGY

6.1 CHARACTERIZATION OF A SELF-RESETTING PULSE GENERATOR FOR USE IN A SUBNANOSECOND FULLY DEPLETED SILICON-ON-INSULATOR CMOS SRAM

An autocorrelator has been designed and fabricated in a 2.0-V, 0.25-μm fully depleted silicon-on-insulator (FDSOI) complementary metal oxide semiconductor (CMOS) process and used to measure the width of pulses emitted from a self-resetting pulse generator, a fundamental element in asynchronous logic design. Variations of the pulse generator are employed in each of the pipeline stages of a subnanosecond asynchronous static random access memory (SRAM) based on the work of Chappell et al. [1],[2]. The autocorrelator is found to be a useful high-speed diagnostic tool that can be implemented in any circuit process.

A schematic of the self-resetting pulse generator is shown in Figure 6-1. The rising edge of an input signal entering the circuit at point A causes a fast pulse—250 ps long for our chip—to emerge at the output at point E. The circuit comprises a feed-forward path in the upper part of the schematic and a reset path in the lower part. The forward path uses three types of transistors: minimum-size static devices (shown in green) used to hold the circuit in its initial state but easily overdriven by other signals, forward devices (shown in red) used to propagate the rising-edge signal to the output, and reset devices (shown in blue) that pull the nodes in the forward path back to their initial states, thereby terminating the pulse. Note that the
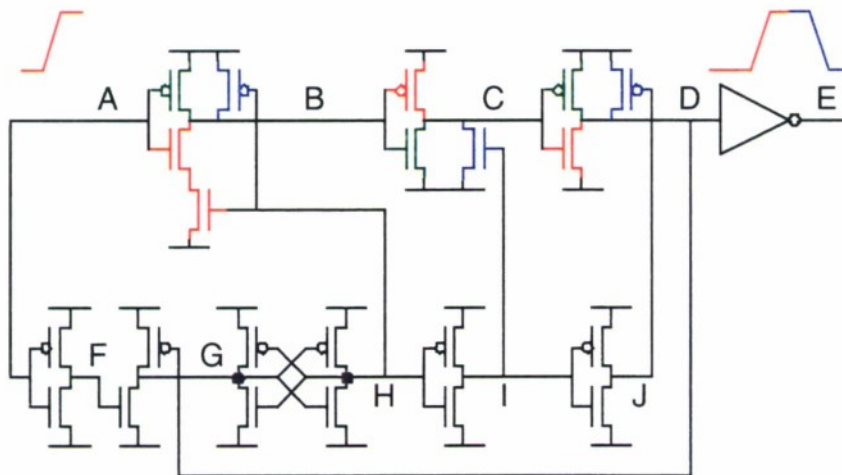
Figure 6-1. Schematic of pulse-generator circuit for which the output pulse width was measured using the on-chip autocorrelator. This circuit was originally developed by Chappell et al. [1],[2]. Three different types of transistors are shown: static devices that hold the circuit in its initial state (green), forward devices that propagate the rising edge through the feed-forward path (red), and reset devices that reset the circuit to its initial state (blue).

feed-forward path is fast compared to standard static logic because the reset devices are turned off while the signal is being fed forward. The forward and reset devices never act on the same node at the same time; hence, the pulse generator has a shorter latency than does standard static logic. This is important in minimizing latency in an SRAM. Moreover, except for the static devices, which are always of minimum size, the transistors all scale up in size from left to right, allowing the pulse generator to drive heavy loads such as the capacitive load of a row or a column in an SRAM array.

The propagation of signals in the circuit is shown in Figure 6-2. Prior to a rising edge at the input (point A), the circuit is in an initial state with the designated circuit nodes at the following voltage levels: B high, C low, D high, E low, F high, G low, H high, I low, and J high. Note that the states of H, I, and J leave the reset devices in the forward path turned off, and the states of B, C, and D are weakly held by the small static devices.

A pulse is initiated by the rising edge of an input signal at point A. This causes the following sequence of events to occur in very rapid succession as the large forward devices shown in red turn on: point B goes low, point C goes high, point D goes low, and point E goes high, marking the beginning of the output pulse.
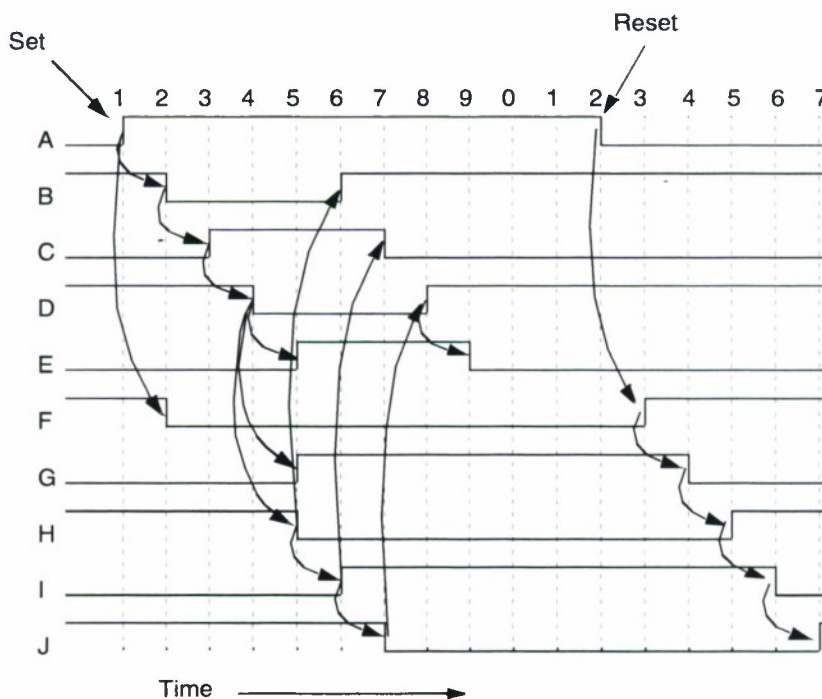
Figure 6-2. Relative timing diagram for the pulse-generator circuit. The signals A through J are labeled in Figure 6-1. The arrows indicate how the signals propagate through the circuit.

When A goes high, it also primes the reset path by driving point F low. This leaves both devices turned off in the inverter between F and G. When the pulse in the forward path reaches D and drives it low, the following sequence of events occurs in rapid succession in the reset path: G goes high, H goes low, I goes high, and J goes low. The outputs from this reset sequence restore the initial conditions in the forward path. Specifically, when point H goes low, the lower pull-down device driving point B is turned off and the reset pull-up device drives B back high. When point I goes high, point C is driven strongly low by the reset device. Similar behavior occurs with the next stage when point J goes low, driving point D back up and terminating the output pulse at point E. The propagation time through the loop from D to G to H to I to J and back to D determines the length of the output pulse.

The final steps in the operation of the circuit occur when the input pulse at point A returns low. In rapid succession, the nodes in the reset path revert to their initial states: F high, G low, H high, I low, J high. This leaves the forward path lightly held in the initial state by the static devices and ready for the rapid propagation of the next pulse.

Figure 6-3 shows the autocorrelator circuit used to measure the pulse width. An off-chip clock, which can be varied from a few hertz to more than 1 GHz, is applied to the circuit. Four inverters, labeled clock cleanup, sharpen the edges and guarantee a clean rising edge to the pulse generator circuit described above. The pulses emitted from the pulse generator enter two parallel chains of 100 CMOS inverters, each of which has a separate power supply for 99 of the inverters, allowing the propagation times to be varied. The two inverter chains thus serve as adjustable delay lines.

The delayed output pulses enter the sampling block, which consists of an n-channel sampling gate (pass gate) followed by three stages of inverting buffers. A pulse that travels through the upper inverter chain is applied to the drain of the sampling transistor and is the signal that is sampled. The pulse that travels through the lower inverter chain is applied to the gate, where it turns on the transistor briefly and allows the signal on the drain to appear at the source. The value of the source signal at the time when the gate pulse ends remains stored on the source capacitance until the next gate pulse occurs. The relative arrival times of the sampled and gating pulses can be adjusted by varying the voltages V_{dd1} and V_{dd2} so that the falling edge of the gating pulse can be made to sweep through the entire sampled pulse to map out its shape.

The lower part of Figure 6-4 shows a photograph of an oscilloscope trace of the output of the autocorrelator with the supply voltage V_{dd1} fixed at 2.0 V while voltage V_{dd2} was oscillated sinusoidally about a dc voltage close to 2 V. The vertical trace is the pulse amplitude at the autocorrelator output, but with the trace inverted to compensate for the inversion introduced by the three inverter stages after the sampler. The autocorrelator was clocked at 4 MHz, and V_{dd2} was varied at a frequency of 40 Hz with a peak amplitude of 50 mV. A 99-stage ring oscillator, assumed to have the same delay as the inverter chains, was used to calibrate the delay vs supply voltage. The measured frequencies of the ring oscillator are shown in Figure 6-5(a); the derived delay times given by $1/(2f)$ are shown in Figure 6-5(b). The top part

49
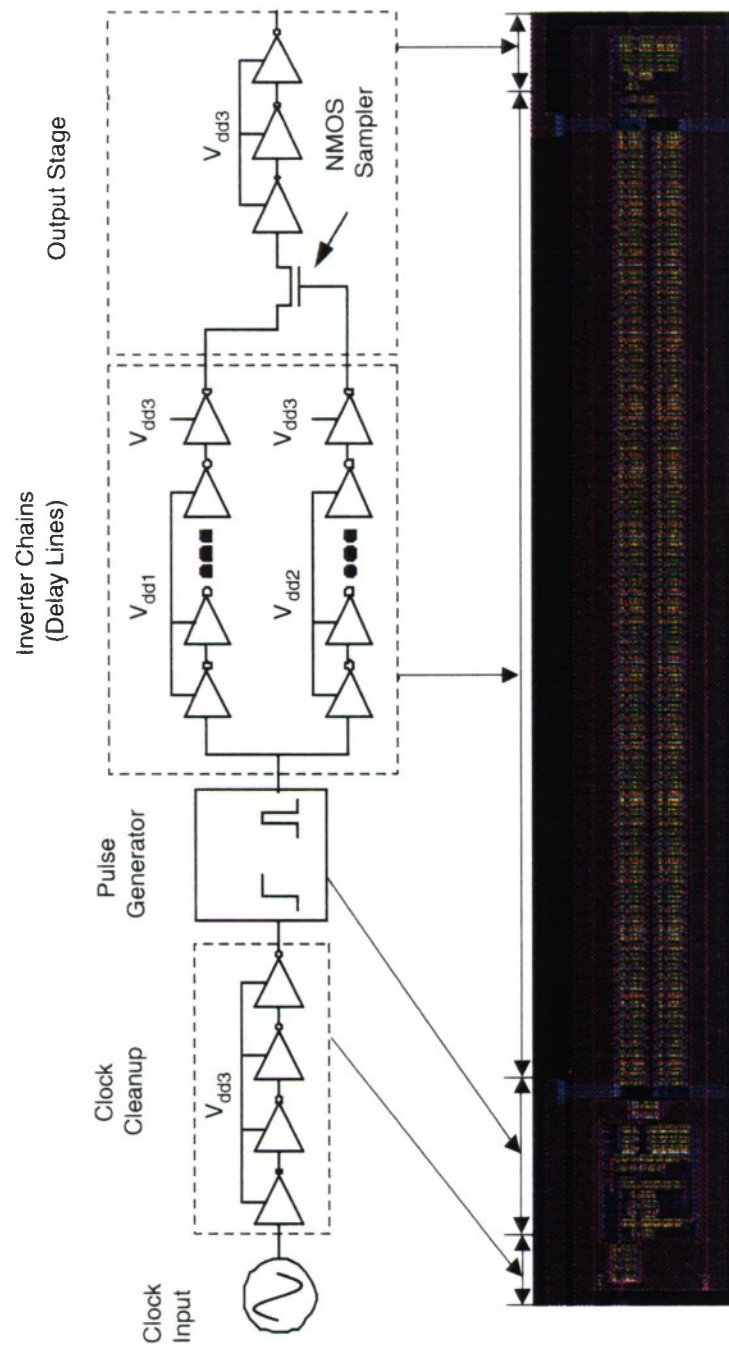
Figure 6-3. Block diagram and corresponding layout of on-chip autocorrelator used to measure the pulse width of a pulse generator circuit.
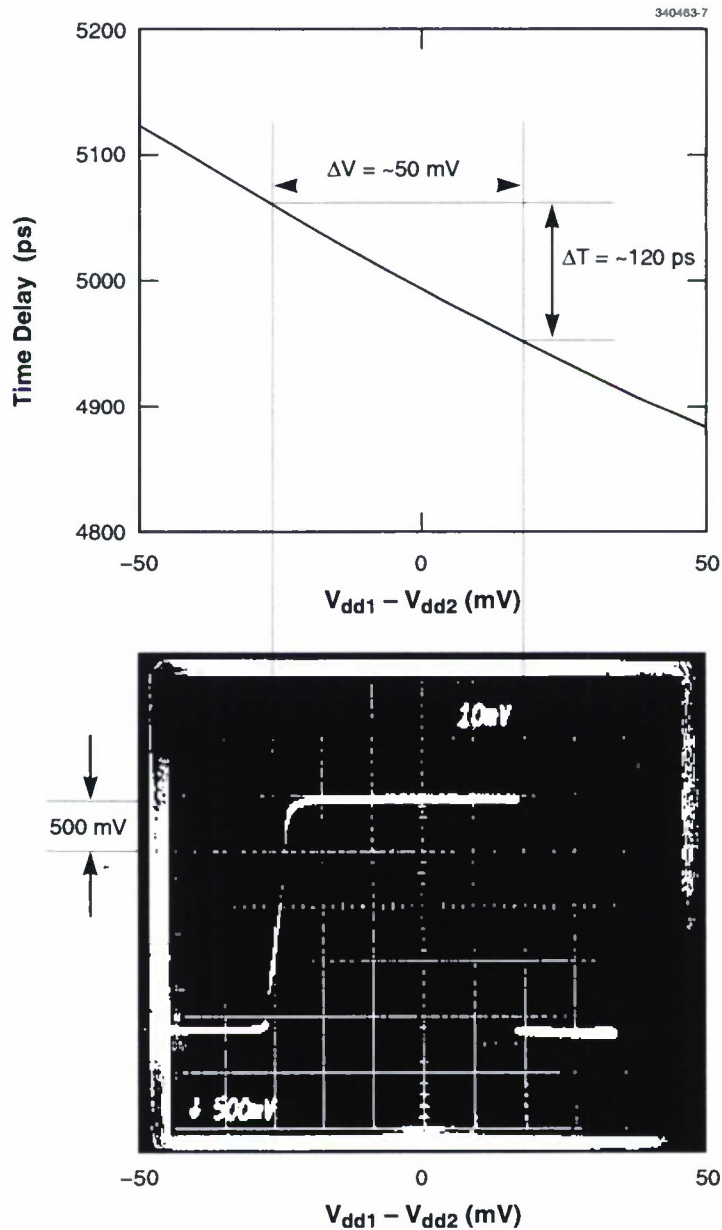
Figure 6-4. Photograph of oscilloscope trace of the output from the autocorrelator circuit. The horizontal axis is the difference voltage ($V_{dd1} - V_{dd2}$). The vertical axis is the amplitude of the pulse. The output has been inverted by the oscilloscope to compensate for the odd number (3) of output buffer inverters. Above the oscilloscope photograph is a voltage-to-time mapping determined by ring oscillator measurements, from which we estimate that the pulse width is ~120 ps.
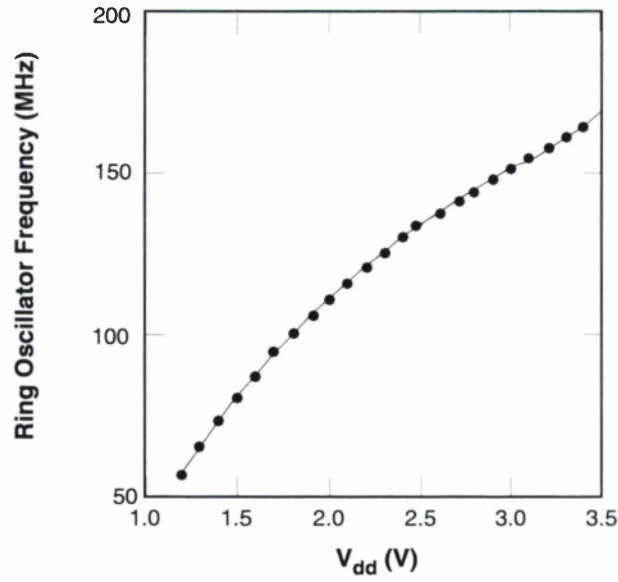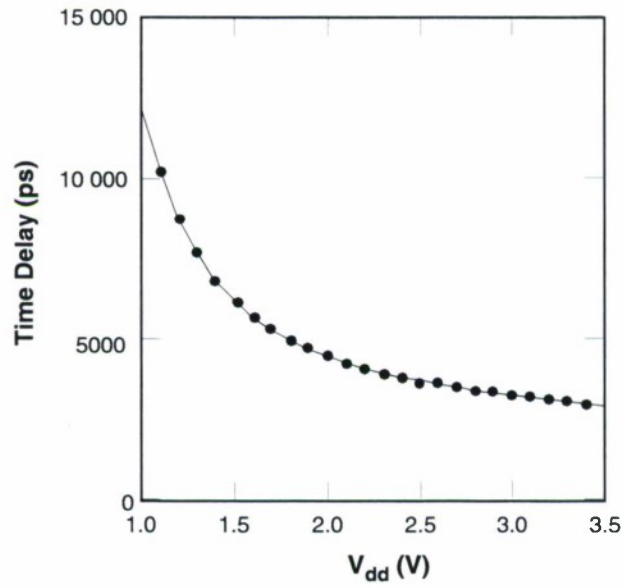
Figure 6-5. (a) Frequency vs voltage of 99-stage ring oscillator found on same chip as autocorrelator. (b) Delay of 99-stage inverter chain, calculated as 1/(2f) from the data in Figure 6-5(a).

52

of Figure 6-4 shows the calibrated delay over the range of the oscilloscope trace. It is interesting to note that the vertical edges of the sampled pulse are sharp to within ±1 mV, corresponding to jitter of less than 4 ps in the delay lines.

Several autocorrelator chips were tested, and the pulse width was always observed to be ~120 ps, significantly shorter than the 250-ps value expected from circuit simulations. Careful simulations of the sampler section of the autocorrelator circuit showed that the output voltage from the sampling transistor was not always reaching the full pulse amplitude of 2.0 V. Several factors contribute to this behavior. When the drain and gate are both at 2V, the source will never rise to more than a threshold drop V_{th} below that. In addition, the transistor's conductance under these conditions will be low, and the time constant to charge the source capacitance will be long. This effect can be seen in the slower rise time compared to the fall time in Figure 6-4. Finally, the negative-going sampling edge of the gate signal will inject charge into the source that will shift its voltage downward. Simulations incorporating these effects show that the output of the sampling gate remains slightly below the 1.0-V threshold of the first inverting buffer over about half the pulse width, and this part of the pulse, consequently, is not seen at the autocorrelator output. Had we used source followers rather than inverters, we would have been able to observe the entire pulse.

The experimental result shown in Figure 6-4 places a lower bound on the pulse width of 120 ps. To place an upper bound on the width, we performed the following experiment: we increased the amplitude of the swing on V_{dd2} to cover a delay range of several nanoseconds, and we increased the input frequency into the range 400 MHz–1 GHz. We could then observe multiple pulses and conclude that the pulse widths were no more than 500 ps.

Using an on-chip autocorrelator circuit, we have determined that a self-resetting pulse generator could generate trains of pulses with a width between 120 and 500 ps and at rates to beyond 1 GHz. The measured jitter between the autocorrelator's two 100-stage inverter chains of less than 4 ps demonstrated that high-precision timing measurements are possible. A small modification to the circuit should allow us to determine precise pulse widths. A variation of the circuit could be used to measure relative timing between any two rising edges in a circuit where precision timing between signals is critical. Our technique is particularly useful as fabrication processes produce smaller, faster transistors for which current picoprobe measurement techniques would introduce excessive loading and would have insufficient bandwidth.

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D. D. Santiago   J. P. Sage

6.2 DEMONSTRATION OF AN 8-kb SUBNANOSECOND SRAM INTEGRATED CIRCUIT DESIGNED ANDFABRICATED IN A 2.0-V, 0.25- μm, FULLY DEPLETED SILICON-ON-INSULATOR CMOS PROCESS

An asynchronously pipelined 8-kb (1 k × 8 b) SRAM containing approximately 60 000 FDSOl CMOS transistors has been demonstrated. The SRAM has been found to function correctly in initial testing at a cycle rate of 10 MHz, and we expect it to be able to cycle at a rate greater than 1.3 GHz.

The goal of this program was to build an SRAM with a modest storage capacity (~8 kb) but achieving subnanosecond access and cycle times and capable of operating at a temperature of 77 K so that it could interface with superconductive electronics operating at 4.2 K. Another constraint was to keep the power dissipation below 1 W to reduce the refrigeration load. A literature search showed that existing research-grade integrated circuits (ICs) did not meet these objectives [3]–[7]. Most were large SRAM arrays that had several-nanosecond access and cycle times. One had subnanosecond access times, but its cycle time was several nanoseconds [7], and it was designed in a BiCMOS process, making operation at 77 K problematic.

We decided that the asynchronous SRAM architecture devised by Chappell et al. was the best design for both fast access and fast cycle times [1],[2]. This design was nearly sufficient to meet our requirements if the transistor gate length was scaled from 0.5 μm down to 0.25 μm, the storage capacity reduced from 512 kb to 8 kb, and the chip fabricated using our FDSOI CMOS process. Simulations showed that these modifications could achieve a 750-ps cycle time and 1.3-ns access time at room temperature. Further speed improvements could be made either by scaling the transistor gate length to below 0.25 μm or by cooling the SRAM to 77 K, where an estimated 30% speed gain could be realized. We estimated that the SRAM would consume less than 0.5 W when operated at a cycle rate of 1 GHz.

Figure 6-6 shows the layout of the 2.2 × 2.2-mm 8-kb SRAM implemented in the Lincoln Laboratory 2.0-V, 0.25-μm FDSOI CMOS process. Figure 6-7 shows a block diagram of the chip. The circuitry surrounding the storage array and used to read from and write to the array is grouped into blocks that are pipelined asynchronously. The chip includes: the SRAM array in which the data are stored in 8192 six-transistor (6-T) memory cells, the row and column decoders and drivers used to select a given byte of memory cells, the write-enable circuitry used either to force SRAM cells into one of two binary states or to read out the binary state of an SRAM cell, and the sense amplifiers that differentially amplify the voltage output of the SRAM cells during a read operation. The input-output (I/O) buffers shown in Figure 6-6 are 32-bit-long shift registers that were included to perform high-speed tests on the SRAM.

Each stage of the pipeline uses asynchronous logic that generates ~250-ps-long pulses and processes data in subnanosecond time intervals. Hence, below several hundred megahertz the circuit behavior is essentially independent of the clock frequency at which the SRAM is cycled. To confirm that the pulse generator circuits operate correctly, we designed and fabricated an on-chip autocorrelator to measure the width of these pulses as described in Section 6.1. We found that the pulse widths were between 125 and 500 ps as required for the SRAM to operate at its intended frequency.

54
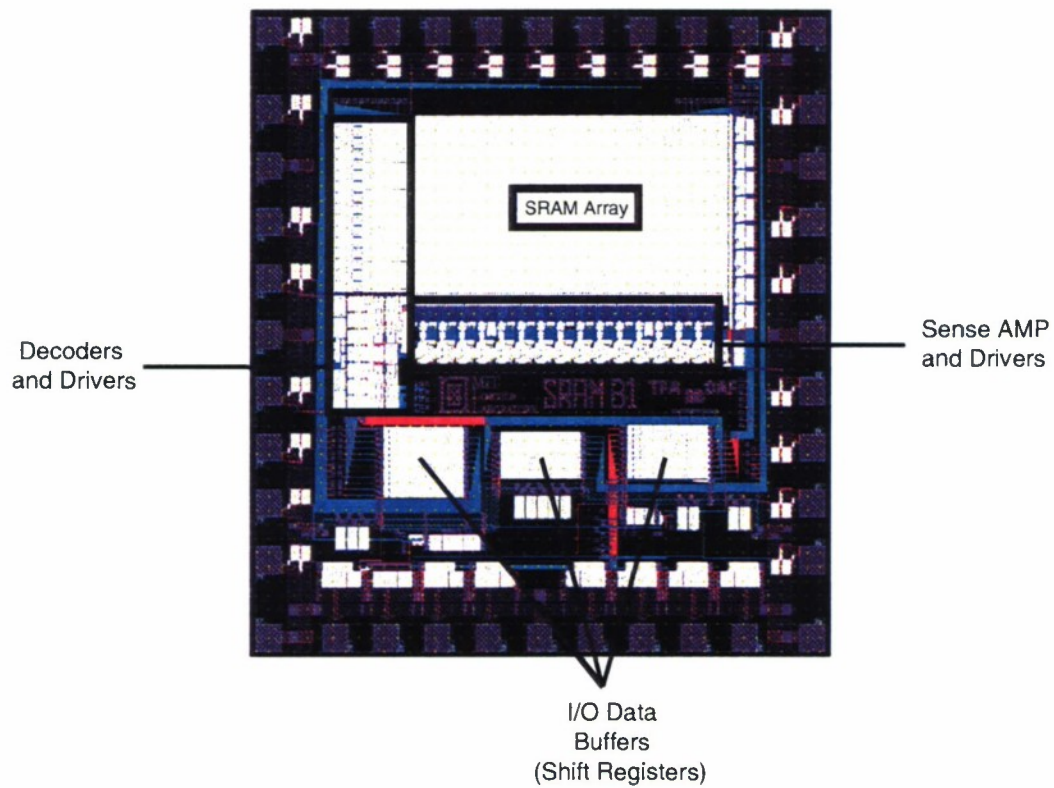
Figure 6-6. Layout of a 2.2 × 2.2-mm 8-kb (1 k × 8 b) SRAM integrated circuit (IC). The IC was designed and fabricated in MIT Lincoln Laboratory's in-house 2.0-V, 0.25-μm, fully depleted silicon-on-insulator (FDSOI) complementary metal oxide semiconductor (CMOS) circuit process.

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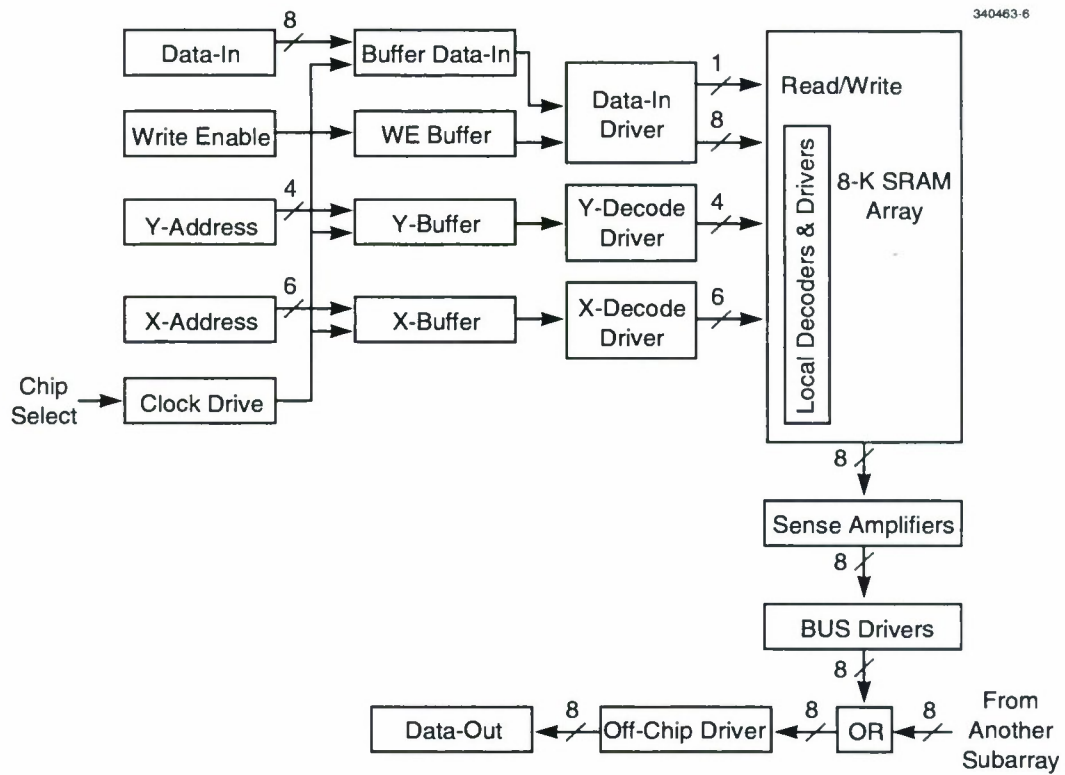
Figure 6-7. Block diagram of the SRAM IC whose layout is shown in Figure 6-6. The circuit blocks shown represent stages of the pipeline.

Figure 6-8 shows the data acquisition system we used to test the SRAM chips. A computer generates a sequence of read/write instructions that is loaded into a word generator. Each read/write instruction consists of a 10-bit address (4 bits to encode 16 rows and 6 bits to encode 64 columns), an 8-bit word containing the data to be written into the SRAM during a write operation, and a write-enable bit that is "high" for a write operation and "low" for a read operation. Once the sequence of instructions has been loaded into the data generator, the data is clocked into the SRAM at a 10-MHz rate. During read operations, 8-bit data words are sent to the SRAM's output port and captured by a digital waveform acquisition system. When the sequence of instructions has been completed, the data stored in the system is downloaded to a computer for analysis.

High-speed testing, to frequencies beyond 1 GHz, was to be performed by loading a set of 32 test words from the word generator into the input shift register at low speed, then running the SRAM at high

speed for 32 cycles using an on-chip clock, and finally reading out the results from the output shift register at low speed. However, a design problem with the on-chip clock generator precluded testing at high speed.

Using the low-speed data acquisition system, we performed two types of tests. In the first, a "diagonal" test, we demonstrated that we could write to the diagonal elements of the SRAM array (a diagonal element is one where the low-order 4 bits of the column address are equal to the 4 bits of the row address). The value 255 (all 8 bits high) was written to the first 16 diagonal elements in the SRAM, and zeros were written to the rest of the memory. Then, all 1-k bytes of the SRAM were read back out. Figure 6-9 shows the results for the first 16×16 block of addresses. The pattern is nearly correct, indicating that we have successfully stored data in the SRAM. Then, zeros were written into the first set of diagonals, and 255 was written into the second set of 16 diagonals. The SRAM was again read out. This process was continued until all diagonal elements had been tested. This test confirmed that we could uniquely address each byte in the SRAM (since every row and every column address had been exercised), that all rows and columns functioned correctly, and that all sense amplifiers were operational.

In the second test, the "counting" test, we incremented a register by 17 and sequentially wrote the value of that register into each of the 1-k addresses in the SRAM. Hence, we wrote the byte pattern 0, 17, 34, 51, ..., 255 into the first 16 addresses. We repeated the pattern until we wrote into all 1024 addresses. Approximately 99% of the bytes read out contained correct values. We found that the SRAM power supply could be varied over a range ± 0.5 V from its nominal 2.0-V operating range without affecting the operation.

In summary, we have designed an 8-kb SRAM that uses a pipelined, asynchronous architecture to achieve subnanosecond access and cycle times for operation at 77 K together with superconductive electronics at 4.2 K. The SRAM was fabricated in the Lincoln Laboratory FDSOI CMOS process and tested at low frequency and room temperature. All elements in the SRAM were demonstrated to function properly. Since the pipelined stages operate with internally generated pulses of ~250-ps width, the low-speed testing confirms that the elements operate at full speed.

D. A. Feld   T. F. Ala'ilima
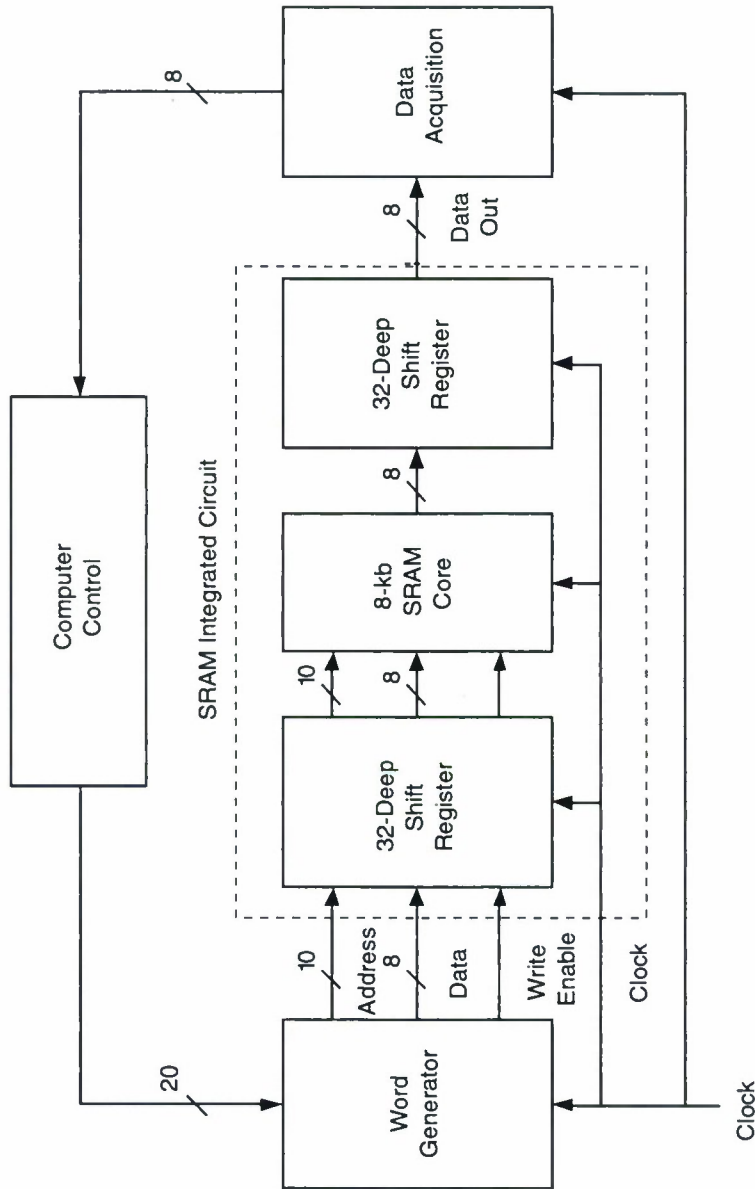R. Berger   T. J. Weir
D. D. Santiago   J. P. Sage

Figure 6-8. Block diagram of low-speed data acquisition test setup used to measure registers were intended for high-speed test. Since the on-chip high-speed clock fai could not be used for high-speed on-chip testing. However, the chip was tested at 1

Column Address

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	255	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	255	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2	0	0	127	0	0	0	0	0	0	0	0	0	0	0	0	0
3	0	0	0	255	0	0	0	0	0	0	0	0	0	0	0	0
4	0	0	0	0	255	0	0	0	0	0	0	0	0	0	0	0
5	0	0	0	0	0	255	0	0	0	0	0	0	0	0	0	0
6	0	0	0	0	0	0	255	0	0	0	0	0	0	0	0	0
7	0	0	0	0	0	0	0	255	0	0	0	0	0	0	0	0
8	255	0	0	0	0	0	0	0	255	0	0	0	0	0	0	0
9	0	0	0	0	0	0	0	0	0	255	0	0	0	0	0	0
10	0	0	0	0	0	0	0	0	0	0	255	0	0	0	0	0
11	0	0	0	0	0	0	0	0	0	0	0	255	0	0	0	0
12	0	0	0	0	0	0	0	0	0	0	0	0	255	0	0	0
13	0	0	0	0	0	0	0	0	0	0	0	0	0	255	0	0
14	0	0	0	0	0	0	0	0	0	0	0	0	0	0	255	0
15	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(Row Address labels 0–15 shown at left.)

Figure 6-9. Results of "diagonal" test in which the memory was filled with 255 (all 8 bits high) for diagonal elements (equal row and column addresses) and zero (all 8 bits low) elsewhere. The 1-k × 8-b SRAM is arranged with 16 rows and 64 columns. Only data in the first 16 columns is shown. This test showed that all of the row and column decoders and sense amplifiers functioned correctly and that most of the SRAM cells were functional.

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7. ADVANCED SILICON TECHNOLOGY

7.1 SUB-100-nm DEEP-ULTRAVIOLET OPTICAL LITHOGRAPHY FOR SILICON-ON-INSULATOR CMOS FABRICATION

The goal of our current sub-100-nm CMOS program is to provide DARPA with a sub-100-nm gate length silicon-on-insulator (SOI) complementary metal oxide semiconductor (CMOS) process for "multiproject" circuit prototyping capability. The first phase of this project involves the transistor engineering required to provide high-performance SOI CMOS at sub-100-nm gate lengths. As part of this effort, we have performed an aggressive gate-only shrink of our 0.25-μm SOI CMOS process. We have developed the lithography and etch processes to enable sub-100-nm gate length SOI CMOS fabrication using conventional deep-ultraviolet (DUV) exposure tools and commercial resists. Our new Canon EX-4, 0.6-NA, 248-nm stepper was employed in this work along with standard commercial resists from Shipley. We were able to achieve resist gate features as small as 50 nm and etched poly features down to 25 nm using a 25-nm etch bias. These feature sizes are near the physical limits of CMOS functionality.

Gate patterns were imaged with a dark-field chromeless phase-shift (DFCPS) approach, illustrated in Figure 7-1. We worked with Numerical Technologies, Inc. (NTI) to extend their dark-field phase-shift method [1] to the chromeless regime, using the gate layer of one of Lincoln's existing multiproject designs. The initial layout, shown in Figure 7-1(a), was used by NTI's proprietary software to generate layout data for two separate reticles. The first, Figure 7-1(b), is mostly chrome (i.e., dark field), with openings only in the vicinity of transistor gates, and phase edges as discussed in the next paragraph. The second, shown in Figure 7-1(c), is a conventional clear-field chrome reticle which is the same as the original layout except that the patterns are bloated somewhat in the vicinity of the transistor gates. To pattern the polysilicon gate layer, both reticles are exposed on the same resist, and the energy in the two aerial images is summed by the resist, shown in Figure 7-1(d), which is then developed. The two reticles were fabricated by a commercial mask-making company.

Reticle 2 produces patterns for polysilicon wiring and any transistors with gates longer than the minimum dimension. Reticle 1 produces only the minimum dimension gates. Inside the windows of reticle 1, a step of the proper height to produce 180° phase shift is etched into the fused quartz material of the reticle. This phase edge causes optical interference, which generates a dark line in the aerial image focused onto the photoresist. The minimum width of the resulting photoresist lines (the gate length) is determined by the exposure dose. In the more common industry practice to date, known as alternating-aperture phase shifting, a minimum-dimension chrome line is also patterned on the reticle next to the phase edge. An important result of the present research is to show that this chrome line is not needed.

The chromeless approach provides superior resolution performance. The absence of minimum-width critical dimensions (CDs) on the reticle simplifies reticle fabrication and minimizes the effects of the mask error enhancement factor (MEEF). MEEF is defined as the wafer error over the mask error multiplied by the stepper reduction factor M:
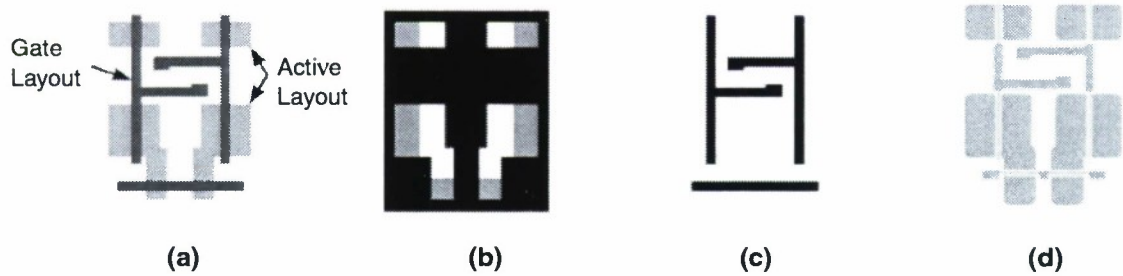
Figure 7-1. Dark-field chromeless phase-shift (DFCPS) lithography.

$$\text{MEEF} = (\partial\text{CD}_{\text{WFR}}/\partial\text{CD}_{\text{MASK}})^*M \ . \tag{7.1}$$

It is important to minimize the MEEF since CD control is becoming increasingly difficult with the growing use of subwavelength imaging approaches.

These reticles are being used to build transistors and integrated circuits and to evaluate the resolution limits, process latitude, and mask topography effects for this lithography method. Figure 7-2 shows a ring oscillator gate pattern with 55-nm resist features over 60 nm of SOI island topography. These features correspond to a k1 factor of 0.13, where k1 is defined by the Rayleigh criterion,

$$\text{Minimum linewidth} = \text{k1} \times \text{wavelength} / \text{numerical aperture (NA)} \ . \tag{7.2}$$

Such features satisfy the 1999 Semiconductor Industry Association (SIA) Roadmap [2] projection for microprocessor gate length in the year 2008. They were imaged using DFCPS with 325 nm of Shipley UV-5 positive photoresist on 62 nm of AR-3 antireflection coating. Our Canon EX-4, 248-nm stepper was employed with partial coherence of 0.3 for the dark-field phase-shift exposure and 0.65 for the bright-field chrome-complement exposure. Figures 7-3(a) and 7-3(b) are resist cross sections for 70- and 50-nm gate features, respectively. Good, high-aspect-ratio sidewall profiles are achieved with this process.

An optimized high-density plasma etch process was developed to transfer these small gate features into polysilicon. This was done on our LAM TCP system utilizing Cl_2 plus HBr chemistries and optical
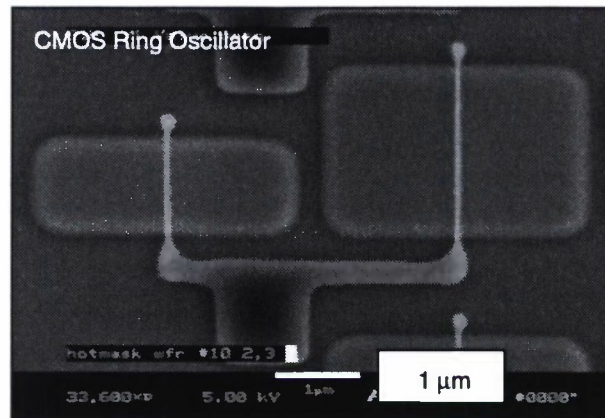
62

Figure 7-2. 55-nm resist gate features on 60-nm silicon-on-insulator (SOI) island topography.

endpointing. The antireflective layer and the underlying polysilicon were etched in the same chamber using a multistep etch process. Excellent sidewall profiles and good selectivity to thin gate oxide were achieved, as shown in Figure 7-4. Figures 7-4(a) and 7-4(b) show scanning electron micrograph (SEM) cross sections of 36-nm polysilicon gratings on a 250-nm pitch. Figure 7-5 shows top-down SEM images of etched gate features on locally thinned SOI islands. Clean pattern transfer of polysilicon gate features down to 25 nm was achieved.

The process latitude for this lithographic approach is large. Figure 7-6 shows a depth of focus (DOF) of ~1 μm achieved for 100-nm gates and 0.7 μm for 60-nm gates. An exposure latitude of 7.6% change in dose for 10% change in linewidth was determined from a power law fit to the CD vs dose data at best focus, as shown in Figure 7-7.

The DFCPS method was also used to pattern dense features in resist. Figures 7-8(a) and 7-8(b) are SEM cross sections of gratings with 250-nm pitch in 255-nm-thick Shipley UV-6 resist. In Figure 7-9(a), a dense grating is resolved, which corresponds to a k1 value of 0.3. This is near the Rayleigh pitch limit of k1 = 0.25 for dense features. The DOF is ~1.0 μm and the exposure latitude ~10%. This capability satisfies the 1999 SIA Roadmap projection for dense line/space features for the year 2003. Figure 7-8(b) shows the same grating imaged at a higher exposure dose yielding 65-nm lines on a 250-nm pitch. The same dose would produce much wider isolated lines owing to optical interference, a result known as the optical proximity effect. To equalize linewidths for dense and isolated structures will require optical proximity correction.

63
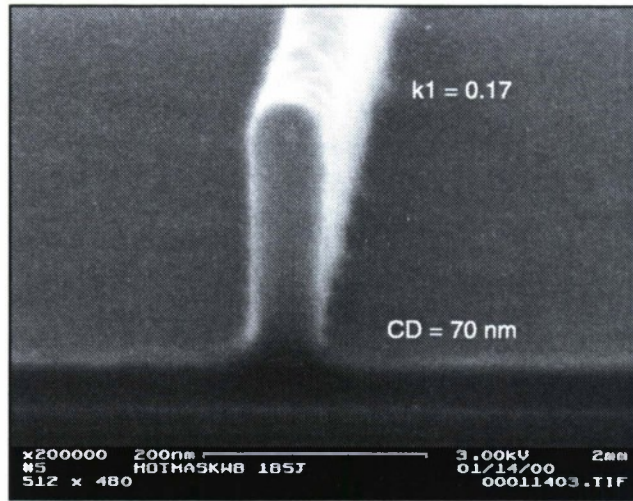
(a)
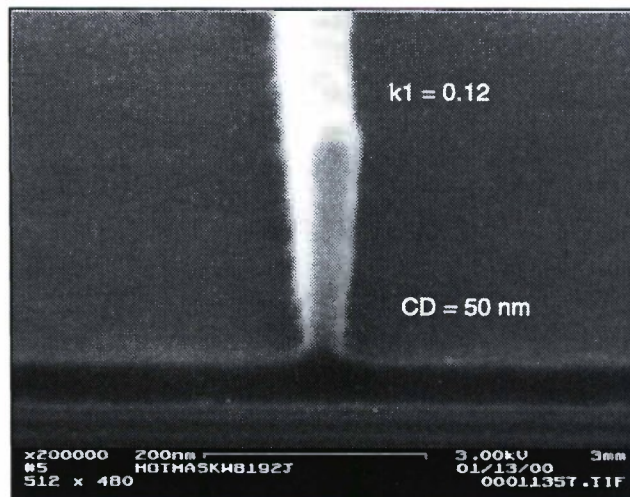
(b)

Figure 7-3. Resist cross sections of (a) 70-nm and (b) 50-nm gate features in Shipley UV-5 photoresist.
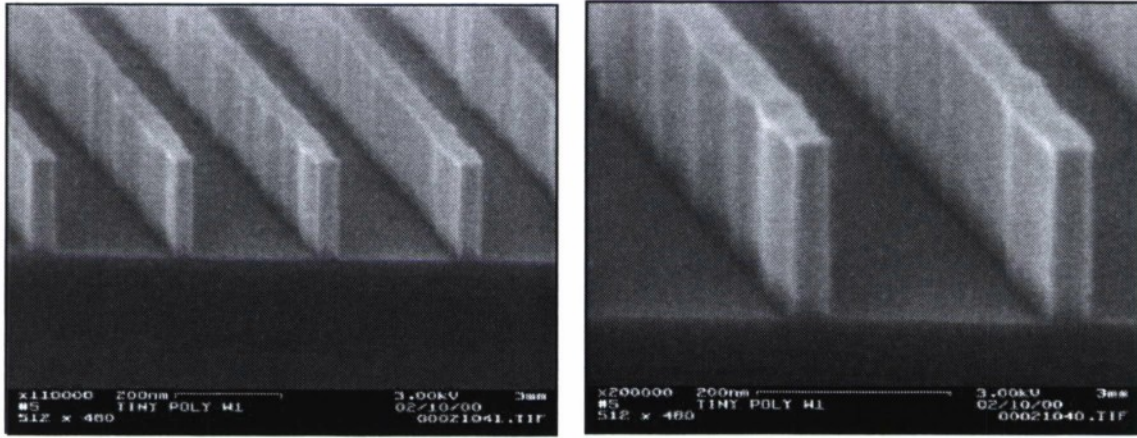
(a)

(b)

Figure 7-4. (a) Polysilicon grating imaged by DFCPS lithography and etched using our new high-density plasma etch process. Critical dimension = 36 nm, and pitch = 250 nm. The etch stopped cleanly on 4-nm gate oxide. (b) 60-nm lines etched into 200-nm-thick polysilicon using a high-density plasma etch process. The etch stopped on a 4-nm gate oxide.
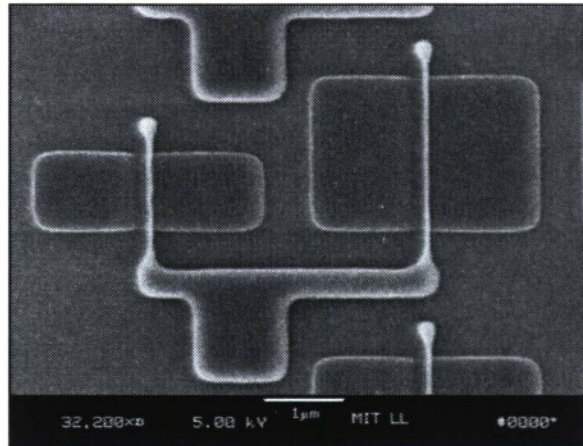
(a)
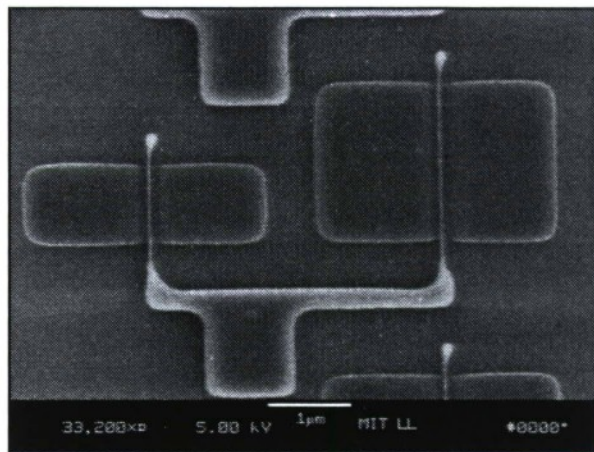
(b)

Figure 7-5. Polysilicon gates on locally thinned SOI islands with (a) 50-nm and (b) 25-nm minimum linewidth.
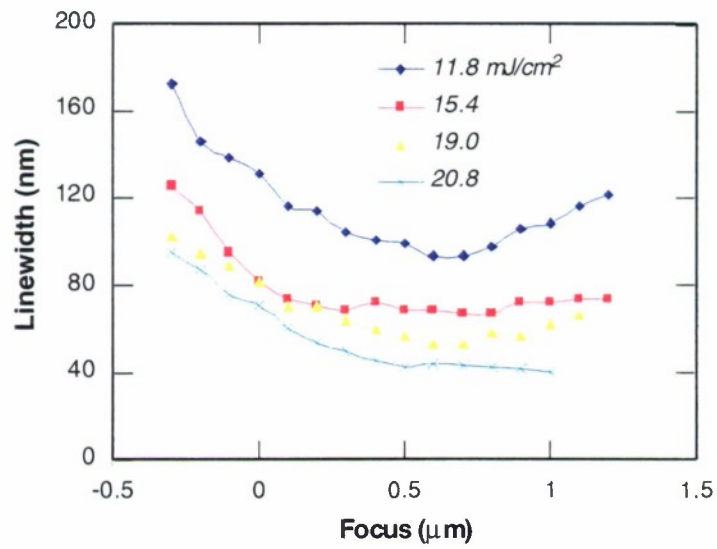
Figure 7-6. Linewidth vs focus for different exposure doses using UV-5 photoresist and AR-3 antireflective coating with DFCPS imaging.
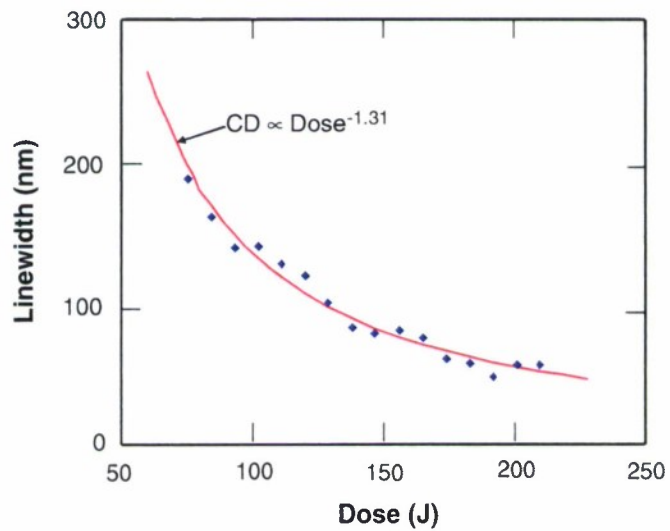
Figure 7-7. Linewidth at best focus vs exposure dose. The fitted curve shows an exposure latitude of 7.6% dose change for 10% linewidth change.
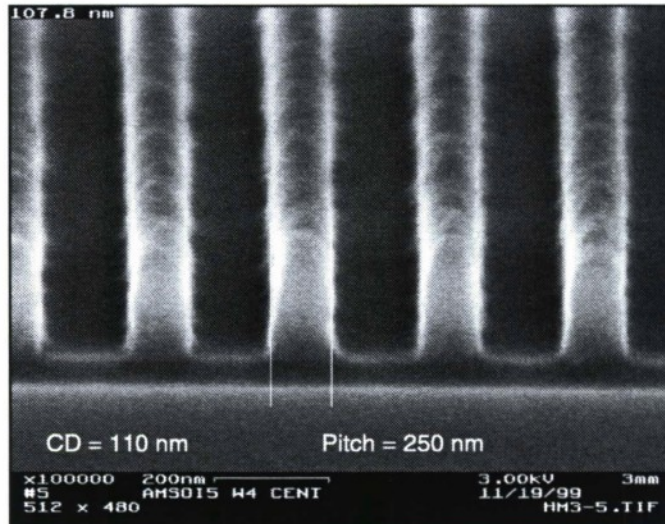
(a)
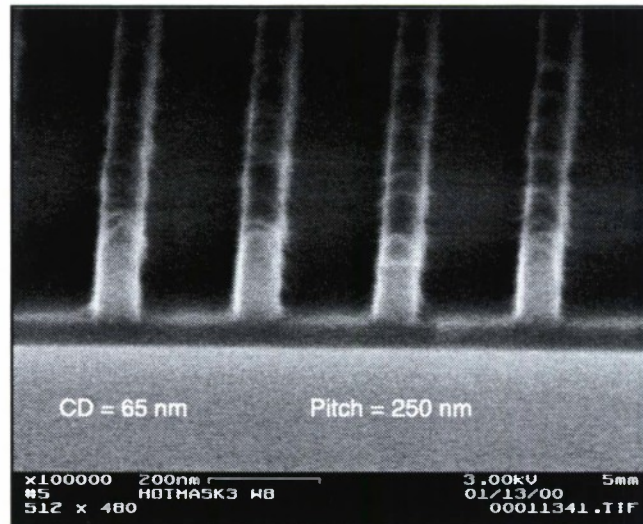
(b)

Figure 7-8. Resist cross sections of dense gratings in UV-6, with linewidth controlled by exposure dose.
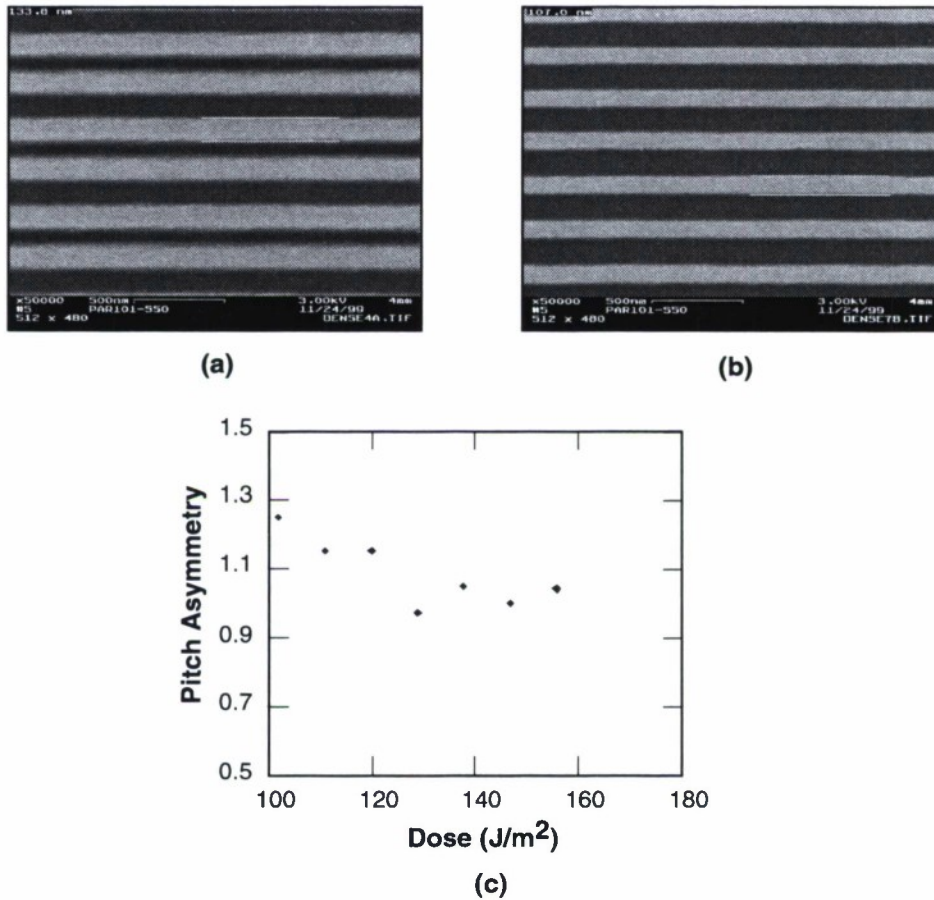
Figure 7-9. (a) Low dose, producing lines wider than spaces, results in pitch asymmetry. No left-right asymmetry is observed. (b) Pitch asymmetry is absent for higher dose in which linewidth is less than spacewidth. (c) Graph of pitch asymmetry vs dose.

Diffraction and scattering associated with mask topography are expected to cause different transmission in the etched and unetched phase-shift mask features. This effect can give rise to pitch asymmetry or left-right linewidth asymmetry. Figure 7-9 shows no linewidth variation, hence no left-right asymmetry, and for the higher dose the pitch is also constant. At the lower dose, which produces wider lines, the spacewidth alternates, an effect known as pitch asymmetry, defined as the ratio of the two alternating pitches. We observe that pitch asymmetry is present only for low dose and is absent for doses where the linewidth is less than the spacewidth, as plotted in Figure 7-9(c).

To summarize, we have extended the dark-field phase-shift mask method to the chromeless regime (DFCPS), and achieved lithography with good process latitudes down to k1 = 0.13 for isolated features and k1 = 0.3 for dense features. These correspond to features sizes of 50 and 125 nm, respectively, for our Canon EX-4, 0.6-NA, 248-nm stepper. This capability satisfies the 1999 SIA Roadmap projections for microprocessor gates in 2008 and dynamic random access memory half-pitch for 2003. We have also developed an advanced polysilicon etch process that has achieved successful pattern transfer for gate features down to 25 nm, near the physical limits of CMOS functionality.

M. Fritze   D. Astolfi
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13. ABSTRACT (*Maximum 200 words*)

This report covers in detail the research work of the Solid State Division at Lincoln Laboratory for the period 1 November 1999–31 January 2000. The topics covered are Quantum Electronics, Electro-optical Materials and Devices, Submicrometer Technology, Biosensor and Molecular Technologies, Advanced Imaging Technology, Analog Device Technology, and Advanced Silicon Technology. Funding is provided by several DoD organizations—including the Air Force, Army, BMDO, DARPA, Navy, NSA, and OSD—and also by the DOE, NASA, and NIST.

14. SUBJECT TERMS

quantum electronics	biosensor technology	microchip lasers	optical lithography
electro-optical devices	advanced imaging technology	avalanche photodiodes	bioelectronic sensors
materials research	analog device technology	wafer bonding	charge-coupled devices
submicrometer technology	advanced silicon technology	stereolithographic patterning	CMOS technology

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